DATA SHEET

GRF6403

31.75 dB RANGE / 0.25 dB STEP DSA
0.05 to 6 GHz

RELEASE Ø DATA SHEET

FEATURES

- 31.75 dB Range
- 0.25 dB Steps via 7-bit Control
- Supports Multiple Control Interfaces — Serial, Direct Parallel and Latched Parallel
- Programmable *Rapid Fire*™ Attenuation Setting Which Circumvents Delays Associated with SPI Programming
- Programmable Defaults for Power-on Resets
- Glitchless Stepping (< 2 dB Over/Undershoot)
- 165 ns Settling Time for 0.25 dB Steps
- Bi-directional RF Use
- 3.3 V and 5 V Supply Voltages
- 50 Ω Single-ended Input and Output Impedances
- -40 to 115 °C Operating Temperature Range
- Compact 4 X 4 mm QFN-24 Package

Reference: 5 V / 2 GHz

- IL: 1.36 dB
- IPO.1dB: 30.4 dBm
- IIP3: 58.9 dBm
- INL Attenuation Error: ± 0.1 dB
- DNL Attenuation Error: ± 0.03 dB

APPLICATIONS

- 5G Wireless Infrastructure
- Cellular Repeaters/Boosters & DAS Systems
- Automotive Cellular and V2X Compensators
- Millimeter Wave IF Stages
- High-performance Gain Trim & AGC Loops
- TDD Applications where a Common DSA is Shared for Both TX and RX Modes of Operation

ORDERING INFORMATION

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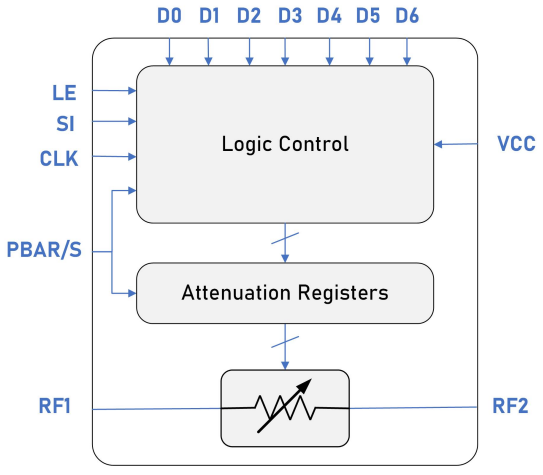
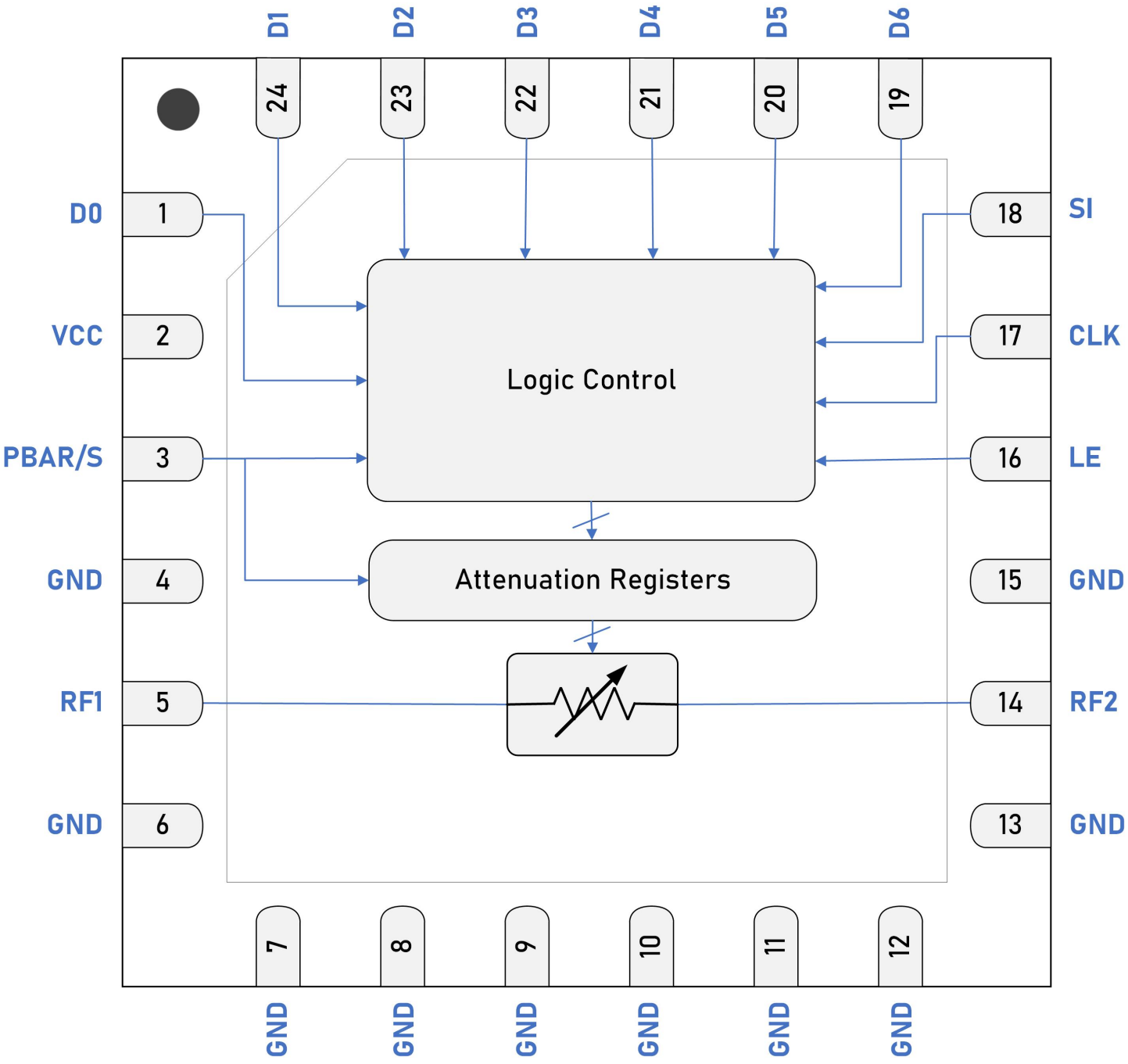
DESCRIPTION

The GRF6403 is a bi-directional, 31.75 dB range digital step attenuator which provides precise stepping in 0.25 dB increments. The device supports three unique programming modes, including serial, direct parallel, and latched parallel. In addition, the GRF6403 includes a special *Rapid Fire*™ attenuation register which allows the device to be immediately switched into a pre-defined secondary attenuation state by toggling a *single* external control line. This ability to quickly shift into an alternative state enables a single device to be used in TDD applications where different attenuation levels are needed for TX and RX modes of operation.

In terms of performance, the GRF6403 can cover the entire 50 MHz to 6 GHz range while still maintaining precise and monotonic gain stepping. Glitching has been minimized to < 2 dB for all steps. The device delivers up to 30.4 dBm of IP0.1dB, 58.9 dBm of IIP3 and a low IL of less than 1.36 dB at 2 GHz.

BLOCK DIAGRAM





Pin Out (Top View)

Pin Assignments

Pin	Name	Description	Note
1	D0	0.25 dB Parallel Control Bit	Pull high to select 0.25 dB attenuation.
2	VCC	V_{CC} Bias Voltage	Connect to V_{CC}. Use bypass capacitors as close to the pin as possible.
3	PBAR/S	Mode Select Pin	If left unconnected, logic will default to HIGH due to included pull-up on chip. **RFA Feature Disabled/Unused:** Logic Low = Parallel Control. Logic High = Serial Control. **RFA Feature Enabled:** Logic Low = Switch in '*Rapid Fire*' attenuation. Logic High = Device reverts back to the previous attenuation state as defined during the last programming sequence. Refer to the programming section for details.
4, 6-13, 15	GND	Ground	Internally grounded. This pin must be grounded with a via as close to the pin as possible.
5	RF1	RF Port 1	Internally matched to 50 Ω. An external DC blocking cap must be used if there is voltage present on the RF line. Since the device supports bi-directional operation, the RF1 port can serve as an input or output.
14	RF2	RF Port 2	Internally matched to 50 Ω. An external DC blocking cap must be used if there is voltage present on the RF line. Since the device supports bi-directional operation, the RF2 port can serve as an input or output.

Pin Assignments (cont.)

Pin	Name	Description	Note
16	LE	Latch Enable	If left unconnected, logic will default to HIGH due to included pull-up on chip. **Serial Mode (PBAR/S = HIGH):** Logic LOW allows data to be shifted in. The logic transition from LOW to HIGH and then back to LOW updates the programming register. **Direct Parallel Mode (PBAR/S = LOW):** For direct parallel mode, keep the LE pin HIGH. Whenever the LE pin is set to logic HIGH, any attenuation value present at the parallel logic pins D[6:0] will be immediately written into the ATTEN[7:0] register. **Latched Parallel Mode (PBAR/S = LOW):** To realize the latched parallel mode, simply toggle the LE pin HIGH and then LOW to latch in the value present at the parallel logic pins D[6:0] into ATTEN[7:0]. Note that while the LE pin is LOW, the data values present on pins D[6:0] have no effect on the ATTEN[7:0] register.
17	CLK	Clock	Serial clock input.
18	SI	Serial Input	Serial data input.
19	D6	16 dB Parallel Control Bit	Pull high to select 16 dB attenuation.
20	D5	8 dB Parallel Control Bit	Pull high to select 8 dB attenuation.
21	D4	4 dB Parallel Control Bit	Pull high to select 4 dB attenuation.
22	D3	2 dB Parallel Control Bit	Pull high to select 2 dB attenuation.
23	D2	1 dB Parallel Control Bit	Pull high to select 1 dB attenuation.

Pin Assignments (cont.)

Pin	Name	Description	Note
24	D1	0.5 dB Parallel Control Bit	Pull HIGH to select 0.5 dB attenuation.
PKG BASE	GND	Ground	Provides DC and RF ground for the device as well as thermal heat sink. Recommend multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page.

Absolute Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	-0.3	6	V
SI, LE, CLK	V_{SPI}	-0.3	6	V
D0, D1, D2, D3, D4, D5, D6, D7, PBAR/S	V_{LOGIC}	-0.3	6	V
Externally Applied DC Voltage to RF1 Pin	V_{RFIN}	-0.3	0.3	V
Externally Applied DC Voltage to RF2 Pin	V_{RFOUT}	-0.3	0.3	V
Short-term Exposure to RF Input Power (RF1 or RF2, Load VSWR = 1:1; Assumes Static State Only; All Attenuation States, V_{CC} = 5V, F_{TEST} ≥ 500 MHz, No Hot Switching, $T_{PKG\ BASE}$ = 25 °C)	$P_{IN\ MAX\ -\ ST}$		32	dBm
Long-term Exposure to RF Input Power (RF1 or RF2, Load VSWR = 1:1; Assumes Static State Only; Max Attenuation State (31.75 dB), V_{CC} = 5.5V, F_{TEST} = 50 MHz, No Hot Switching, $T_{PKG\ BASE}$ = 105 °C)	$P_{IN\ MAX\ -\ LT}$		26.5	dBm
Operating Temperature (Package Base)	$T_{PKG\ BASE}$	-40	115	°C
Maximum Junction Temperature	T_{J-MAX}		125	°C
Electrostatic Discharge				
Charged Device Model	CDM	750		V
Human Body Model	HBM	1		kV
Storage				
Storage Temperature	T_{STG}	-65	150	°C
Moisture Sensitivity Level	MSL		1	-

Caution! ESD Sensitive Device.

Exceeding Absolute Maximum Rating conditions may cause permanent damage.

Note: For additional information, please refer to Manufacturing Note MN-001 - Packaging and Manufacturing Information.

All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging. For additional information, please refer to the Certificate of RoHS Compliance.

Recommended Operating Conditions

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Power Supply Voltage	V_{CC}	3	5	5.5	V	
Operating Temperature Range	$T_{PKG\ BASE}$	-40		+115	°C	Measured on Package Heat Sink
RF Frequency Range **(Note 1)**	F_{RF}	0.05		6	GHz	
RF Input Power @ $T_{PKG\ BASE}$ < 105 °C (Static States)	P_{IN-MAX}			26	dBm	Static attenuation state; all state changes occur in the absence of any RF power being applied to the device. $T_{PKG\ BASE}$ < 105 °C.
RF Input Power @ $T_{PKG\ BASE}$ < 105 °C. (Hot Switching)				20		Hot switching condition; state changes can occur at any time while RF power is applied to the device. $T_{PKG\ BASE}$ < 105 °C.
RF1 Port Impedance	Z_{RF1}		50		Ω	Single ended
RF2 Port Impedance	Z_{RF2}		50		Ω	Single ended

Note 1: Operation outside of this range is possible, but with degraded performance of some parameters.

Nominal Operating Parameters - General

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Logic Input Low	V_{IL}	0		0.63	V	
Logic Input High	V_{IH}	1.17		V_{CC}	V	
Logic Current	I_{IL}, I_{IH}		12.5		µA	V_{CC}=5 V, $T_{PKG\ BASE}$=105 °C.
5 V Supply Current	I_{CC-5V}		260		µA	Static operation
3.3 V Supply Current	$I_{CC-3.3V}$		220		µA	Static operation
Serial Clock Speed	f_{CLK}			30	MHz	
LE to First Serial Clock Rising Edge	t_{LS}	10			ns	50% of LE falling edge to 50% of CLK rising edge.
Serial Data Hold Time	t_H	10			ns	50% of CLK rising edge to 50% of data falling edge.
Final Serial Clock Rising Edge to LE	t_{CLS}	10			ns	50% of CLK rising edge to 50% of LE rising edge.
DSA Settling Time	t_{ADJ}		133		ns	Any adjacent step (50% of LE to within 0.1 dB of the final value.)
	$t_{MAX-MIN}$		418		ns	Max to min attenuation (50% of LE to within 0.1 dB of the final value.)
	$t_{MIN-MAX}$		668		ns	Min to max attenuation (50% of LE to within 0.1 dB of the final value.)

Thermal Data

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Thermal Resistance (Infrared Scan)	Θ_{JC}		39		°C/W	On standard evaluation board. Max attenuation state.

Nominal Operating Parameters - General

Thermal Data (Cont.)

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Junction Temperature @ $T_{PKG\ BASE}$ = +115 °C	$T_{J\ @\ 115°C}$		125		°C	V_{CC}=5.5 V, F_{TEST}=50 MHz, Max Attenuation (31.75 dB), P_{IN}=24 dBm, CW.
Junction Temperature @ $T_{PKG\ BASE}$ = +105 °C	$T_{J\ @\ 105°C}$		115		°C	V_{CC}=5.5 V, F_{TEST}=50 MHz, Max Attenuation (31.75 dB), P_{IN}=24 dBm, CW.

Nominal Operating Parameters - RF

The following conditions apply unless noted otherwise: typical application schematic, V_{CC} = 5 V, 50 Ω system impedance, F_{TEST} = 2.0 GHz, $T_{PKG\ BASE}$ = 25 °C. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Attenuation Range	G_{RANGE}		31.75		dB	
Attenuation Resolution	G_{STEP}		0.25		dB	
Over/Undershoot During Step Transition	$G_{OVER/UNDER}$		< 2		dB	Any step
Step Error Between Any Two Adjacent States	DNL		±0.01		dB	0.05 GHz ≤ F_{RF} ≤ 1 GHz
			±0.02			1 GHz ≤ F_{RF} ≤ 2 GHz
			±0.03			2 GHz ≤ F_{RF} ≤ 3 GHz
			±0.08			3 GHz ≤ F_{RF} ≤ 4 GHz
			±0.09			4 GHz ≤ F_{RF} ≤ 5 GHz
			±0.10			5 GHz ≤ F_{RF} ≤ 6 GHz
Absolute Attenuation Error at 0.5 GHz	$INL_{0.5GHz}$		0.05		dB	Atten=6 dB
			0.05			Atten=10 dB
			0.09			Atten=18 dB
			0.09			Atten=24 dB
			0.13			Atten=30 dB
Absolute Attenuation Error at 1 GHz	$INL_{1\ GHz}$		0.05		dB	Atten=6 dB
			0.04			Atten=10 dB
			0.09			Atten=18 dB
			0.09			Atten=24 dB
			0.12			Atten=30 dB
Absolute Attenuation Error at 2 GHz	$INL_{2\ GHz}$		0.04		dB	Atten=6 dB
			0.04			Atten=10 dB
			0.09			Atten=18 dB
			0.08			Atten=24 dB
			-0.11			Atten=30 dB

Nominal Operating Parameters - RF

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Absolute Attenuation Error at 2.5 GHz	$INL_{2.5\ GHz}$		0.04		dB	Atten=6 dB
			0.04			Atten=10 dB
			-0.09			Atten=18 dB
			-0.07			Atten=24 dB
			-0.1			Atten=30 dB
Absolute Attenuation Error at 3.55 GHz	$INL_{3.55\ GHz}$		0.05		dB	Atten=6 dB
			-0.05			Atten=10 dB
			-0.1			Atten=18 dB
			-0.08			Atten=24 dB
			-0.1			Atten=30 dB
Absolute Attenuation Error at 4.7 GHz	$INL_{4.7\ GHz}$		0.04		dB	Atten=6 dB
			-0.04			Atten=10 dB
			-0.08			Atten=18 dB
			-0.04			Atten=24 dB
			-0.1			Atten=30 dB
Absolute Attenuation Error at 6 GHz	$INL_{6\ GHz}$		-0.04			Atten=6 dB
			-0.04			Atten=10 dB
			-0.06			Atten=18 dB
			-0.15			Atten=24 dB
			-0.16			Atten=30 dB
Relative Phase Between the MIN and MAX Attenuation States	Φ_{Δ}		7		°	F_{RF}=0.5
			14.3			F_{RF}=1 GHz
			28.3			F_{RF}=2 GHz
			34.6			F_{RF}=2.5 GHz
			48			F_{RF}=3.55 GHz
			62.5			F_{RF}=4.7 GHz
			74.6			F_{RF}=6 GHz

Nominal Operating Parameters - RF

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Adjacent Step Phase Deviation at 0.5 GHz	$ASPD_{0.5\ GHz}$		0.13		°	Atten=6 dB
			0.11			Atten=10 dB
			0.18			Atten=18 dB
			0.46			Atten=24 dB
			0.4			Atten=30 dB
Adjacent Step Phase Deviation at 1 GHz	$ASPD_{1\ GHz}$		0.21		°	Atten=6 dB
			0.22			Atten=10 dB
			0.18			Atten=18 dB
			0.33			Atten=24 dB
			0.46			Atten=30 dB
Adjacent Step Phase Deviation at 2 GHz	$ASPD_{2\ GHz}$		0.43		°	Atten=6 dB
			0.48			Atten=10 dB
			0.66			Atten=18 dB
			1.21			Atten=24 dB
			0.54			Atten=30 dB
Adjacent Step Phase Deviation at 2.5 GHz	$ASPD_{2.5\ GHz}$		0.57		°	Atten=6 dB
			0.62			Atten=10 dB
			0.82			Atten=18 dB
			1.46			Atten=24 dB
			1.05			Atten=30 dB
Adjacent Step Phase Deviation at 3.55 GHz	$ASPD_{3.55\ GHz}$		0.88		°	Atten=6 dB
			0.97			Atten=10 dB
			1.22			Atten=18 dB
			2.0			Atten=24 dB
			1.14			Atten=30 dB

Nominal Operating Parameters - RF

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Adjacent Step Phase Deviation at 4.7 GHz	$ASPD_{4.7\ GHz}$		1.23		°	Atten=6 dB
			1.33			Atten=10 dB
			1.63			Atten=18 dB
			2.56			Atten=24 dB
			1.48			Atten=30 dB
Adjacent Step Phase Deviation at 6 GHz	$ASPD_{6\ GHz}$		1.65		°	Atten=6 dB
			1.73			Atten=10 dB
			2.12			Atten=18 dB
			3.2			Atten=24 dB
			2.01			Atten=30 dB
Insertion Loss	S21, S12		1.11		dB	F_{RF}=0.5 GHz
			1.18			F_{RF}=1 GHz
			1.36			F_{RF}=2 GHz
			1.47			F_{RF}=2.5 GHz
			1.71			F_{RF}=3.55 GHz
			2.18			F_{RF}=4.7 GHz
			2.84			F_{RF}=6 GHz
Gain Flatness Over any 200 MHz Band	$S21_{FLAT}$		0.07		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			0.07			2 GHz ≤ F_{RF} ≤ 3 GHz
			0.07			3 GHz ≤ F_{RF} ≤ 4 GHz
			0.07			4 GHz ≤ F_{RF} ≤ 5 GHz
			0.07			5 GHz ≤ F_{RF} ≤ 6 GHz
Gain Variation Over Temp	$S21_{TEMP}$		+0.35/-0.25		dB	$T_{PKG\ BASE}$=-40 to 115 °C, Referenced to $T_{PKG\ BASE}$=25 °C

Nominal Operating Parameters - RF

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
RF Port 1 Return Loss Over all Attenuation Settings	S11		> 24		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			> 25			2 GHz ≤ F_{RF} ≤ 3 GHz
			> 21			3 GHz ≤ F_{RF} ≤ 4 GHz
			> 17			4 GHz ≤ F_{RF} ≤ 5 GHz
			> 15			5 GHz ≤ F_{RF} ≤ 6 GHz
RF Port 2 Return Loss Over All Attenuation Settings	S22		> 22			0.05 GHz ≤ F_{RF} ≤ 2 GHz
			> 22			2 GHz ≤ F_{RF} ≤ 3 GHz
			> 20			3 GHz ≤ F_{RF} ≤ 4 GHz
			> 17			4 GHz ≤ F_{RF} ≤ 5 GHz
			> 15			5 GHz ≤ F_{RF} ≤ 6 GHz
Input 3rd Order Intercept ATTN = 0 dB, Over Frequency **(Note 2)**	IIP3		54.3		dBm	F_{RF}=0.5 GHz
			58.5			F_{RF}=1 GHz
			58.9			F_{RF}=2 GHz
			58.1			F_{RF}=2.5 GHz
			58.9			F_{RF}=3.55 GHz
			62.6			F_{RF}=4.7 GHz
			59.8			F_{RF}=6 GHz
Input 3rd Order Intercept F_{RF} = 2 GHz, Over Attenuation **(Note 3)**	IIP3		58.9		dBm	ATTN=0 dB
			56.8			ATTN=15.75 dB
			55			ATTN=31.75 dB
Input 0.1 dB Compression ATTN = 0 dB, Over Frequency	$IP_{0.1dB}$		30.2		dBm	F_{RF}=0.5 GHz
			30.4			F_{RF}=1 GHz
			30.4			F_{RF}=2 GHz
			31.2			F_{RF}=2.5 GHz
			31			F_{RF}=3.55 GHz
			31			F_{RF}=4.7 GHz
			31.9			F_{RF}=6 GHz

Note 2: 18 dBm P_{OUT} per tone at 2 MHz spacing.
Note 3: 19 dBm P_{IN} per tone at 50 MHz spacing.

Nominal Operating Parameters - RF

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Input 0.1 dB Compression F_{RF} = 2 GHz, Over Attenuation	$IP_{0.1dB}$		30.4		dBm	ATTN=0 dB
			29.6			ATTN=12 dB
			29.9			ATTN=18 dB
Maximum Non-RF Driven Spurious Over Rated Frequency Range of 50 MHz to 6 GHz **(Note 4)**	$SPUR_{MAX}$		-114		dBm	F_{RF}=50 MHz to 65 MHz
			-120			F_{RF}=65 MHz to 115 MHz
			-125			F_{RF}=115 MHz to 6 GHz

Note 4: Spurious due to on-chip negative voltage generator. Typical fundamental frequency is approximately 10 MHz. Measured at either RF port when externally terminated into 50 Ω.

Functional Description

The GRF6403 employs several programming options to control the device's digital step attenuator. Parallel programming is supported via the device's 7 external control pins. Alternatively, the device can be programmed using an enhanced 3-wire SPI (serial-parallel interface). As a supplement to its traditional serial programming, the GRF6403 also includes a *Rapid Fire*™ selection mode which allows the device to be immediately switched into a pre-defined attenuation state. The following sections provide specific details on each programming mode.

Direct Parallel Programming

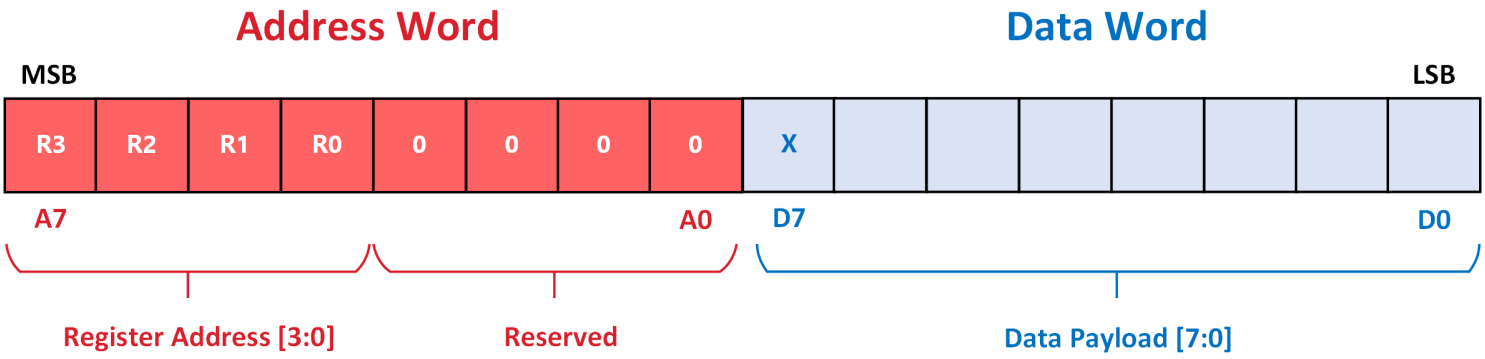
To use the direct parallel programming mode, simply apply a logic LOW to the PBAR/S pin while simultaneously keeping the LE pin HIGH. When the LE pin is set to logic HIGH, any attenuation value present at the parallel logic pins D[6:0] will be immediately written into the ATTEN[7:0] register.

Latched Parallel Programming

To realize the latched parallel mode programming, set PBAR/S to logic LOW; toggle the LE pin HIGH and then LOW to latch in the value present at the parallel logic pins D[6:0] into ATTEN[7:0]. Note that while the LE pin is LOW, the data values present on pins D[6:0] have no effect on the ATTEN[7:0] register.

Serial Programming

A 16-bit SPI transaction is required to program the GRF6403. Information is shifted in with the least significant bit (LSB) first. Refer to the figure below for an overview of the relevant bit assignments:

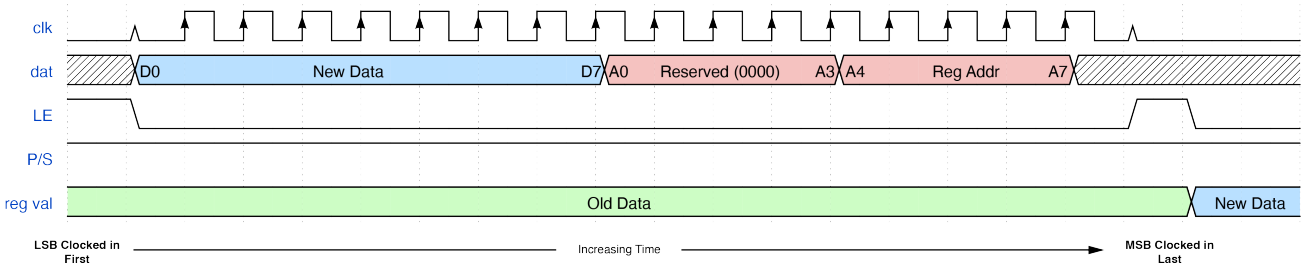


16-Bit SPI Transaction Payload Diagram

Per the diagram above, the payload consists of two separate 8-bit words. The data word is clocked in first. ***Bit D7 is reserved; program in a "0" or a "1" for each SPI transaction.*** Bits D6-D0 make up the 7-bit data payload. Note that the data payload will vary depending upon the register being targeted with the write command; *separate 16-bit SPI transactions are therefore required for programming each of the device's three registers.*

The address word is clocked in next, and it includes two separate bit fields. Bits A7-A4 identify the desired register address. **Bits A3-A0 are reserved and must be programmed with a "0000" during each 16-bit SPI transaction.**

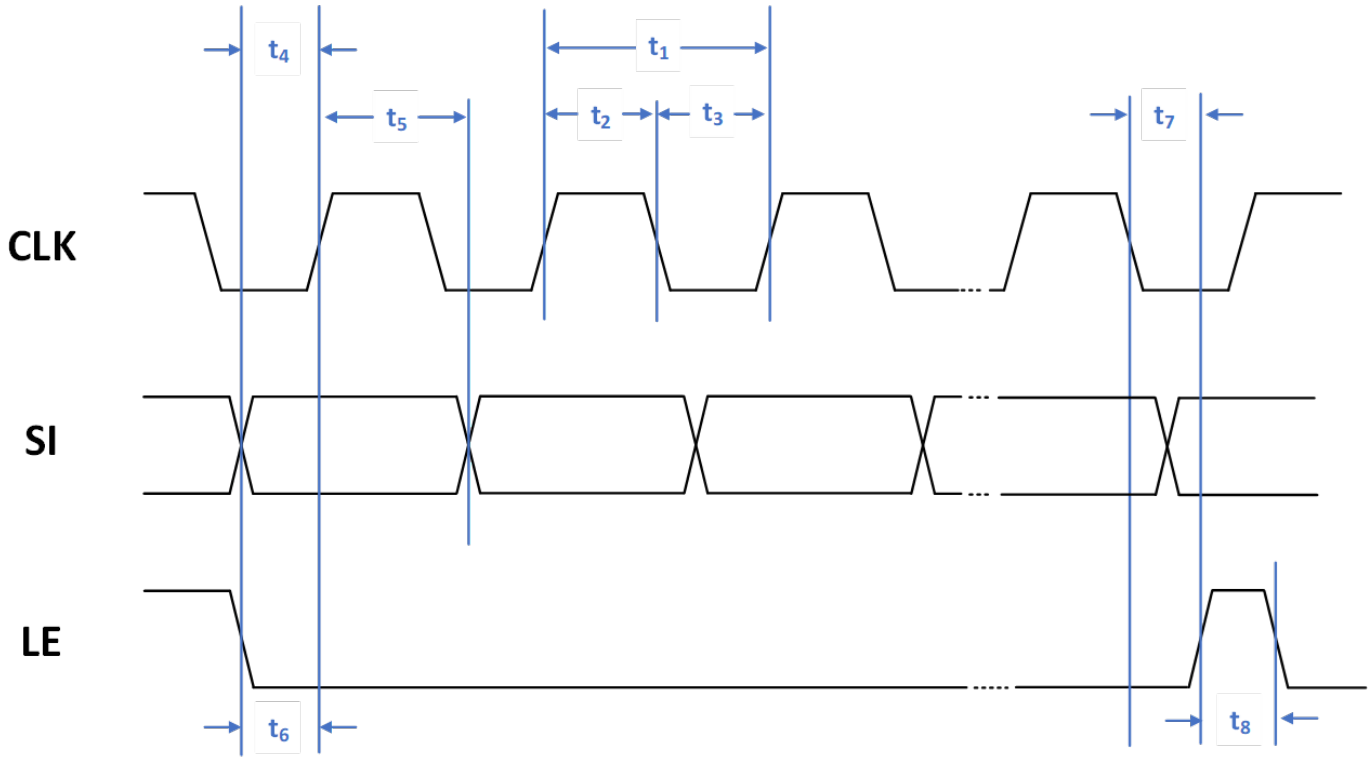
The figure below depicts the timing associated with each programming sequence.



16-Bit SPI Programming Sequence

The sequence begins when the latch enable (LE) line is pulled LOW. After clocking in all 16 bits of the SPI payload, ***an LE line transition to HIGH and then back to LOW will latch bits D7-D0 into the addressed register. This latching process is completed as soon as LE transitions back to LOW.***

SPI Timing Intervals



SPI Timing Diagram

SPI Timing Specifications

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Serial Clock (CLK) Speed	f_{CLK}			30	MHz	
CLK Period	t1	33.3			ns	
CLK High Duration Time	t2	16.7			ns	
CLK Low Duration Time	t3	16.7			ns	
SI to CLK Setup Time	t4	10			ns	
SI Hold Time	t5	10			ns	
LE Low Setup Time	t6	10			ns	
LE High Setup Time	t7	10			ns	
LE High Time	t8	10			ns	

Register Mapping

The GRF6403 includes 3 separate 8-bit registers which help to facilitate the device's various programming functions. The first register, **ATTEN,** is used to set the device's attenuation state when operated in its normal serial mode. Upon all power-on resets (PORs), the register defaults to [01111111], meaning that the attenuator will be set to its maximum attenuation state.

The **CONFIG** register is used to activate the RFA feature. Upon PORs, all bits within the register will default the 0s. thus placing the RFA feature in a disabled state. If the user decides to employ the RFA option, then the [1] bit field must be set to '1' with a separate SPI transaction.

The third register, **RFAREG**, is tied to the GRF6403's *Rapid Fire™ Attenuation* feature. As with the ATTEN register, the RFAREG will default to its maximum attenuation state for all POR conditions. Subsequent SPI programming transactions allow the user to set this register to any customized state between 0 and 31.75 dB. The bit assignments within this particular register get passed along to the attenuator core whenever the RFA feature is enabled AND the external PBAR/S pin (pin 3) goes LOW.

The remaining registers are unused, and they should NOT be written to with any SPI transaction.

Detailed Register Map

Register Address	Name	Width	Description	Bit Fields	POR Value
0x0	ATTEN	8 bits	Attenuator state when in serial mode.	**[6:0]:** DSA Attenuation Word [1111111] = Max Atten [1000000] = Half Max Atten [0000000] = Min Atten **[7]:** *Unused; can be set to **0** or **1***	[01111111]
0x1	CONFIG	8 bits	Stores configuration settings	**[0]:** *Rapid Fire™ Pointer Flag* **0 =** RFA attenuation is set from RFAREG **1 =** RFA attenuation is set from the logic present on the external D0 - D6 pins **[1]:** *Rapid Fire™ Feature On/Off Selection* **0** = RFA Disabled **1** = RFA Enabled **[7:2]:** *Unused; all bits can be set to **0** or **1***	[00000000]
0x2	RFAREG	8 bits	Stores value for Rapid-Fire mode attenuation	**[6:0]:** RFA (*Rapid Fire™* Attenuation) Word [1111111] = Max Atten [1000000] = Half Max Atten [0000000] = Min Atten **[7]:** *Unused; can be set to **0** or **1***	[01111111]
0x3-0xF	Unused	8 bits	Do not write to these registers		[00000000]

Register Truth Tables

The following truth pertain to the attenuator words as used within the ATTEN and RFAREG register.

7-Bit SPI Word Bit Assignments

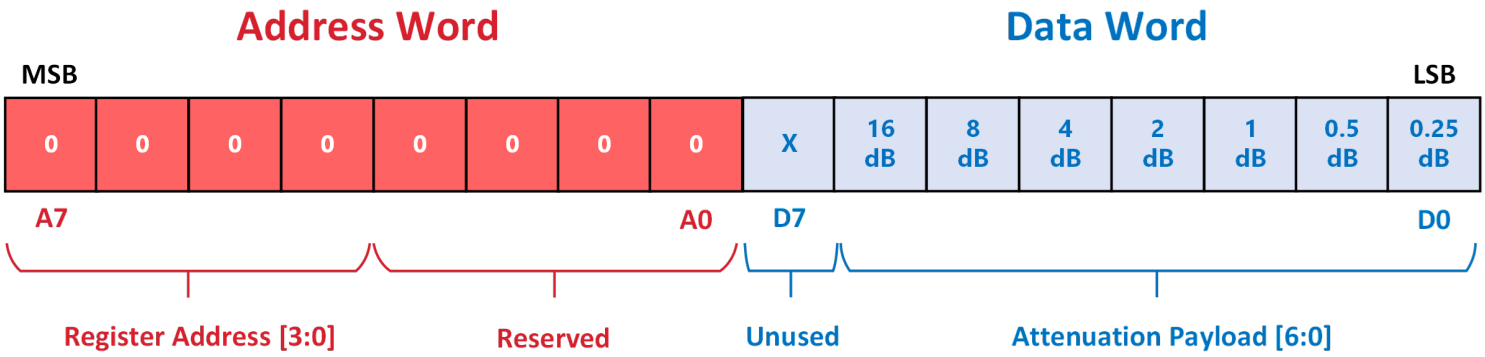
Data Bit	Attenuation Control
D7	Not Used
D6	16 dB Attenuator Control
D5	8 dB Attenuator Control
D4	4 dB Attenuator Control
D3	2 dB Attenuator Control
D2	1 dB Attenuator Control
D1	0.5 dB Attenuator Control
D0	0.25 dB Attenuator Control

Serial Control Word Abbreviated Truth Table

Attenuation	D7	D6	D5	D4	D3	D2	D1	D0
0 dB	X	0	0	0	0	0	0	0
0.25 dB	X	0	0	0	0	0	0	1
0.5 dB	X	0	0	0	0	0	1	0
1 dB	X	0	0	0	0	1	0	0
2 dB	X	0	0	0	1	0	0	0
4 dB	X	0	0	1	0	0	0	0
4 dB	X	0	1	0	0	0	0	0
16 dB	X	1	0	0	0	0	0	0
31.75 dB	X	1	1	1	1	1	1	1

Basic DSA serial programming

Upon power-on / reset (POR), the GRF6403 will default to an attenuation setting of 31.75 dB. A simple SPI command can then be executed to change this attenuation setting by writing directly to the device's ATTEN register (0x0). Be sure to include the relevant '0s' noted in the diagram below for bits A3-A0. Bit D7 is unused, and it can be assigned a '0' or '1' logic. Apply the relevant attenuation bits within the data word per the truth tables provided above.

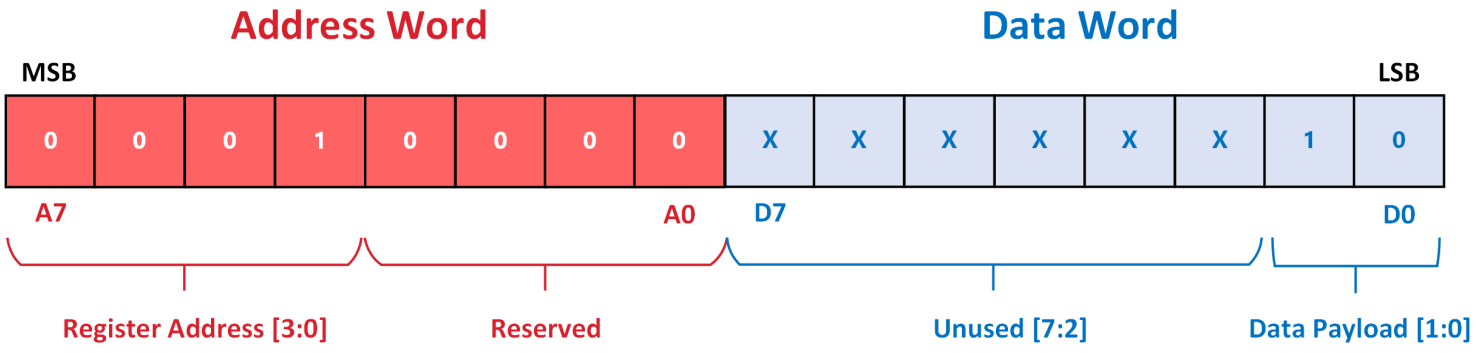


16-Bit SPI Payload for Basic DSA Programming

Rapid Fire™ Attenuation (RFA) Feature

The RFA feature enables the user to quickly switch the attenuator into a pre-defined state, thus circumventing the delays commonly associated with serial programming. A single control line allows the user to rapidly toggle between two attenuation states. In essence, the RFA feature provides a hybrid control mechanism which combines the speed of parallel programming with the convenience of a single control line. This form of control is useful for a multitude of applications where this fast switching is crucial for protecting downstream stages from overexposure to excessively large RF signals. This ability to quickly shift into a secondary state also allows a single device to be used in TDD applications where different attenuation levels are needed for RX and TX applications.

To use the GRF6403's RFA feature, a one-time SPI command must first be sent to the device to activate the feature set. (Note that any subsequent PORs will also require the user to re-activate the RFA feature; PORs force the CONFIG register to revert to its default setting, and the RFA is de-activated as part of this default).



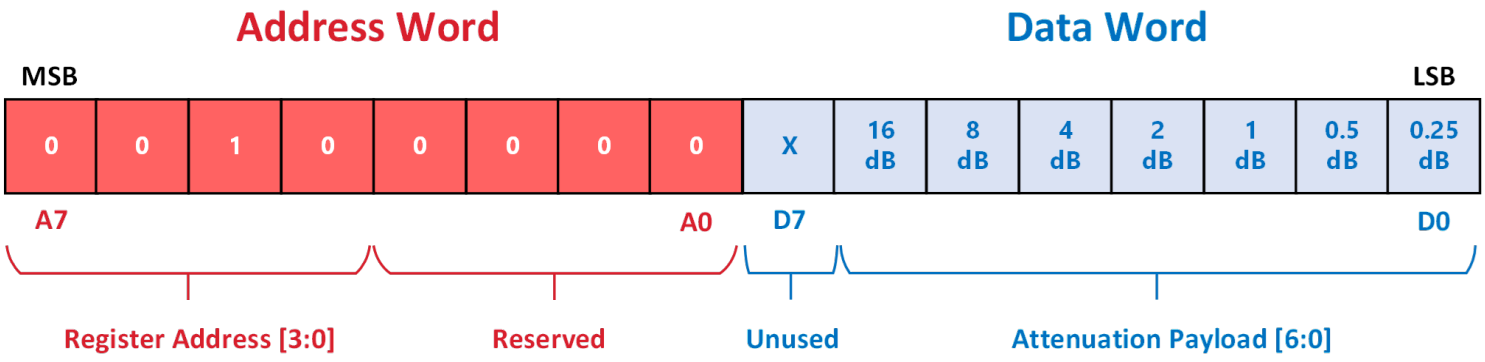
16-Bit SPI Payload for Activating the RFA Feature

Be sure to include the relevant '0s' noted in the diagram for bits A3-A0. Bits D7-D2 are unused and can be assigned a '0' or '1' logic. D1 is set to '1' to activate the RFA feature. ***Note that bit D0 determines the 'source' for the Rapid Fire™ attenuation value.*** Setting D0 to '0' instructs the device to pull the attenuation setting directly from the RFAREG whenever the RFA feature is activated. Conversely, setting D0 to '1' tells the device to pull the attenuation setting from the logic present on the external D0 - D6 pins. This added flexibility is useful in cases where one might want to hardwire in the amount of *Rapid Fire™* attenuation. One such application is described below in the section entitled *Setting Customized Attenuation Levels for Power on Resets (PORs)*.

To deactivate the RFA feature, simply perform an identical SPI transaction, but set D1 to '0' instead.

Once the feature is enabled, simply toggle the logic on the PBAR/S pin (pin 3) to switch between the attenuation settings stored in registers *ATTEN* (0x0) and the chosen *Rapid Fire™* Attenuation 'source' (i.e. *RFAREG* (0x2) or the logic present on the external D0 - D6 pins). A logic 'LOW' switches in the attenuation settings from the chosen RFA 'source', and a logic 'HIGH' reverts back to the previous attenuation state in the ATTEN register as defined during the last programming sequence.

To customize the amount of attenuation being 'fired in', an additional SPI command must also be sent to change the RFA level from its default of 31.75dB. Simply perform a separate SPI transaction to write to the RFAREG:



16-Bit SPI Payload for customizing the RFA's Attenuation Setting

As mentioned earlier, be sure to include the '0s' noted in the diagram for bits A3-A0. Apply the relevant attenuation bits within the data word per the truth tables provided above.

Setting Customized Attenuation Levels for Power on Resets (PORs)

Under normal *Power-on Reset (POR)* conditions, the GRF6403 will load in a default attenuator setting of 31.75 dB (i.e. full attenuation, defined by the default ATTEN register setting of 01111111). If needed, an alternative POR attenuation setting can be obtained by utilizing the logic present on the GRF6403's external parallel programming pins. The following procedure outlines an application technique for realizing these customized POR attenuation levels.

Step 1: Set the desired POR attenuation logic on the GRF6403's external *parallel programming pins (D0-D6)*

There are two options available for setting this logic. If the intent is to exclusively use the SPI interface for your dynamic DSA programming, then the simplest approach is to *hardwire* the device's parallel bits to your desired default POR attenuation state. Directly connect pins D0 to D6 to either VCC or GND to match the desired attenuation logic combination.

Alternatively, use pull-ups/pull-downs on each pin to set the desired logic. If the intent is to connect the GRF6403's parallel pins to the system's microcontroller, then using pull-ups/pull-downs is the only viable implementation available.

Step 2: At Power On, Invoke the *Direct Parallel Programming Mode*

When the part is first turned on, invoke the direct parallel programming mode by assigning a logic HIGH to the LE pin and a logic LOW to the PBAR/S pin. Doing so will automatically apply the attenuator logic that is present on the external parallel bits, thus overriding any of the defaults in the ATTEN register. Consider using external pull-ups/pull-downs on the LE and PBAR/S pins, respectively, if you are uncertain about the default POR logic sourced by your microcontroller.

Step 3: Choose a Programming Mode

Option A: Transition to *Serial Programming Mode*

After start-up, transition to the serial programming mode by changing the logic on the PBAR/S pin to HIGH. (This will, of course, require a dedicated control line from your microcontroller to the PBAR/S pin.) After selecting the serial programming mode, proceed with programming the GRF6403 with the required 16-bit SPI transaction.

Option B: Stay in Parallel Programming Mode

Alternatively, after start-up, stay in the *Direct Parallel* or *Latched Parallel* Programming Mode by keeping PBAR/S at a logic LOW. For *Latched Parallel* Programming, use the LE pin as a toggle to latch in the logic present on the GRF6403's D0 – D6 programming pins. The external D0 – D6 pull-ups/pull-downs implemented for the POR will then be overridden with subsequent parallel logic applied by the microcontroller.

Step 4: Activate the RFA Feature (if desired for Serial Programming operation)

Remember that the RFA (*Rapid Fire*™ Attenuation) mode is disabled on PORs. To engage the RFA feature, go through the initialization steps associated with your first 16-bit SPI transaction. If desired, the hardwired logic on the external D0 - D6 pins can be used as the 'source logic' for determining the RFA level. In this instance, changing the [0] bit field in the CONFIG register to a '1' will direct the RFA to toggle between the attenuation logic present within the ATTEN register and the hardwired logic present on the external D0 - D6 pins.

Using the GRF640x DSA Control GUI

Requirements

Windows PC with the following:

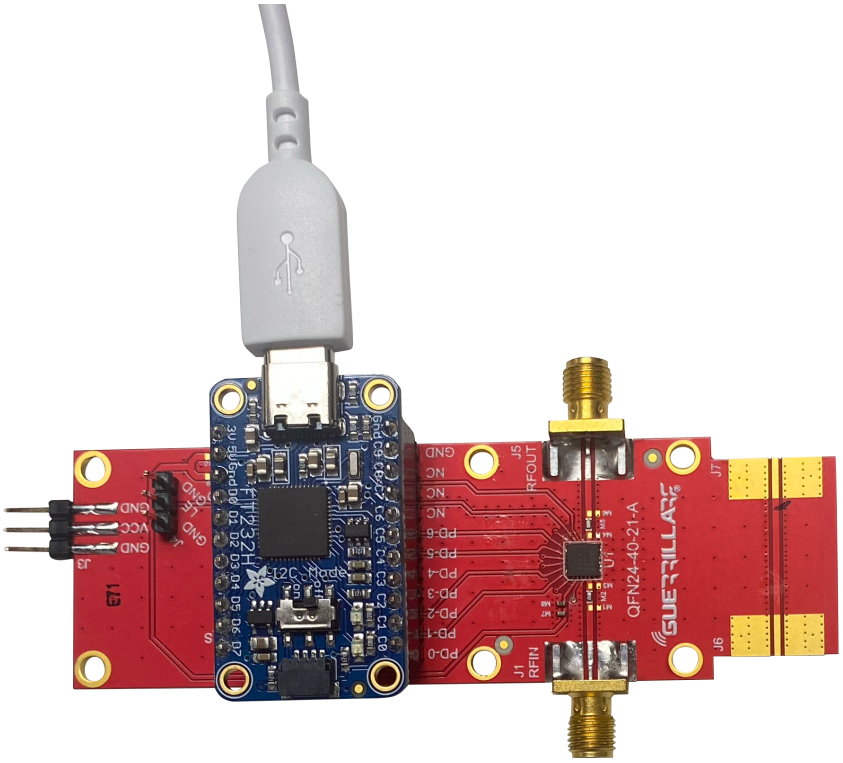
- Windows 10 (or newer) operating system. (Note: the GUI will not run on Mac OS or Linux machines.)
- USB-C capability (either native or via a USB-A to USB-C adapter)

GRF Control GUI

- Executable GUI Application File (.exe)
- GUI can be downloaded directly from the 'Applications' tab within the GRF6403 product page. Click here to access the page within Guerrilla RF's website.

Overview

The GRF6403 evaluation board is designed to work in conjunction with the *Adafruit FT232H USB_C to GPIO, SPI, and I2C Controller.* This separate breakout board attaches directly to the GRF6403's QFN24-40-21-A evaluation board as shown below. After downloading the GRF DSA control software, any USB-C equipped PC running Windows 10 (or newer) can be used to activate the control panel GUI. Please note that more in-depth programming details can be found in the "Detailed Register Map" section of this datasheet.



The evaluation board is connected to an Adafruit breakout board that uses a USB-C port.

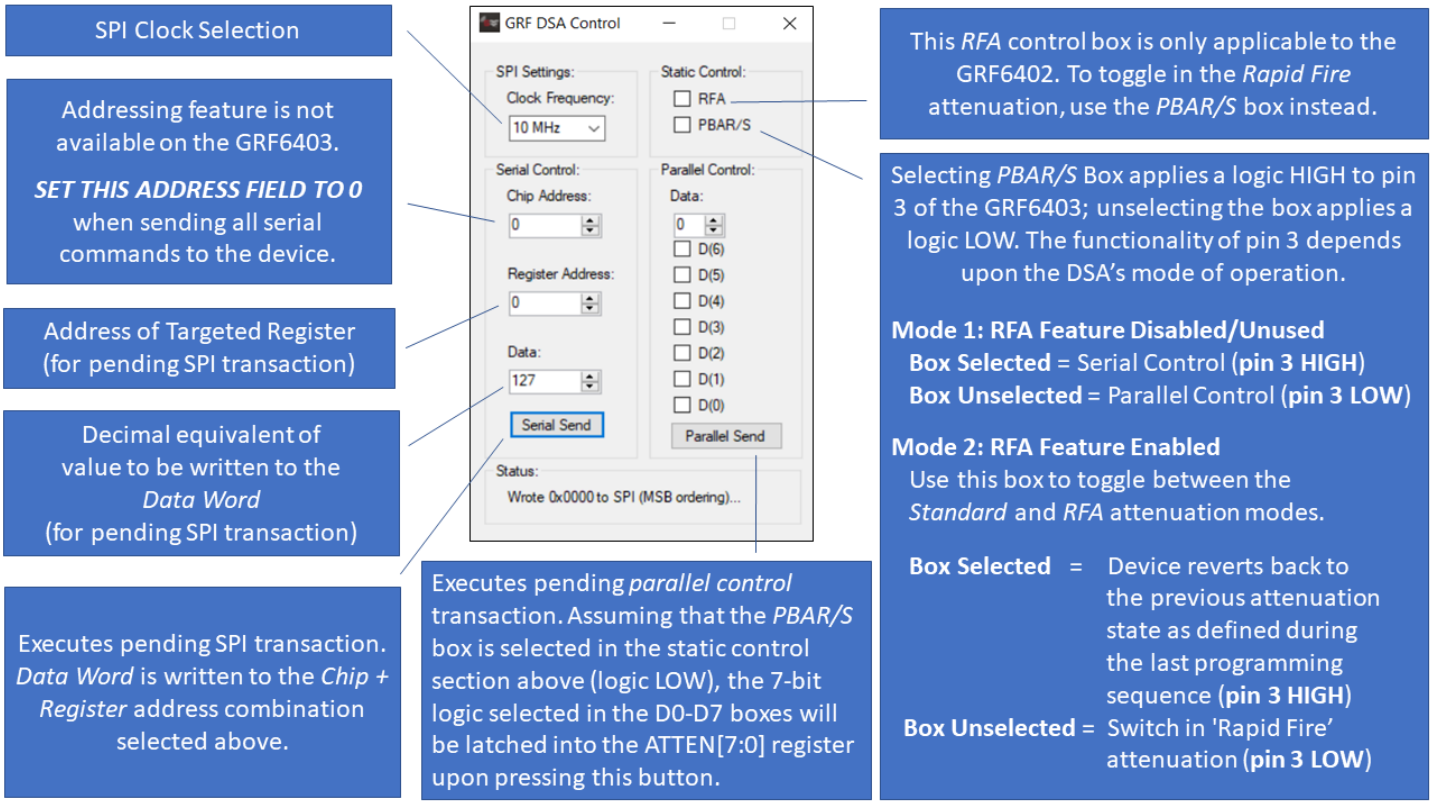
Getting Started

After downloading the GUI control application onto your PC, simply follow the steps below to initiate communication between your PC and the GRF6403 evaluation board.

1. Connect the Adafruit controller to your computer via any USB-C connection. The appropriate drivers for the controller should load automatically for PCs running Windows 10 or 11.
2. To activate the "GRF DSA Control" GUI, launch the executable called "grf_dsa_gui.exe."

Note: Since the GUI is an executable file, your PC's security software may prevent you from simply downloading and running the application without some form of override or intervention. Review the instructions associated with your preferred security software to allow the executable to launch.

Once launched, the GUI application will reveal the control panel shown below.



The DSA Control Panel

Selectable Control Options

SPI SETTINGS

Clock Frequency

- Use the pull-down menu to select from a set of pre-determined frequencies ranging from 1 MHz to 30 MHz.

SERIAL CONTROL

Chip Address

- This entry automatically formats the three address bits (A0-A2) used within the 16-bit SPI transaction.
- For the GRF6403, the chip's internal address has been hardcoded to '0'. **As such, a *Chip Address* of '0' must be used in order to execute all SPI commands using this GUI.**

Register Address

- This entry selects the targeted register to be written to with the pending SPI transaction.
- Select from one of 3 possible addresses.
  - Address 0: ATTN register
  - Address 1: CONFIG register
  - Address 2: RFAREG register

Data

- Use this entry to program bits D0-D7 (the data word) for the pending SPI transaction.
- Select from one of 128 possible word combinations.
  - 0 = x0000000
  - 127 = x1111111

Serial Send

- Ensure that the PBAR/S box is CHECKED within the "Static Control" field prior to executing all serial commands.
- Click on the "Serial Send" button when ready to execute the SPI transaction.
- All data present within the "Chip Address," "Register Address" and "Data Fields" will be formatted and sent to the GRF6403 via a 16-bit word.

STATIC CONTROL

- Use the "Static Control" boxes to select the logic on the RFA (applicable for the GRF6402) and PBAR/S (applicable for the GRF6403) pins.

- RFA Logic Assignments **(Applicable to the GRF6402 Only)**
  - RFA box *SELECTED*: Logic HIGH assigned to pin 11 on the GRF6402 [RFA attenuation (from Register 2) Switched In]
  - RFA box *UNSELECTED*: Logic LOW assigned to pin 11 on the GRF6402 [Primary Attenuation (from Register 0) Switched In]

- PBAR/S Logic Assignments **(Applicable to the GRF6403 Only)**
  - PBARS/S box *SELECTED*: Logic HIGH assigned to pin 3
  - PBARS/S box *UNSELECTED*: Logic LOW assigned to pin 3

  Note that the functionality of the PBAR/S pin depends upon the DSA's mode of operation:

  Mode 1: RFA Feature Disabled/Unused
  When the RFA feature is disabled, use the PBAR/S box to switch between basic serial and parallel control.
  Box *SELECTED* = Basic Serial Control Enabled (pin 3 HIGH)
  Box *UNSELECTED* = Basic Parallel Control Enabled (pin 3 LOW)

  Mode 2: RFA Feature Enabled
  Use the PBAR/S box to toggle between the *Standard* and *RFA* attenuation modes.
  The RFA feature must first be enabled within the CONFIG register to realize this functionality.

  Box *SELECTED* = Switch in the 'Standard/Primary' attenuation (pin 3 HIGH)
  Box *UNSELECTED* = Switch in 'Rapid Fire' attenuation (pin 3 LOW)

  Note: The 'Rapid Fire' attenuation is defined as the attenuation level programmed into
  the RFA register OR the level determined by the logic present on the external D0-D6 pins.
  The 'source' of the 'RFA' attenuation is defined by the 'pointer' bit within the CONFIG register.
  Refer to the RFA feature section above for details.

PARALLEL CONTROL (Applicable to the GRF6403 Only)

Data

- Use this entry to program in the external logic for bits D0-D6 (pins 1, 24, 23, 22, 21, 20 and 19).
- Select from one of 128 possible word combinations.
  - 0 = x0000000
  - 127 = x1111111

Parallel Send

- Ensure that the PBAR/S box is left *UNSELECTED* within the "Static Control" field prior to executing all parallel commands.
- Select the desired logic for bits D0-D6.
- Click on the "Parallel Send" button when ready to apply the parallel logic to pins 1, 24, 23, 22, 21, 20 and 19.

Changing the Attenuation Level within the ATTEN Register

1. To make any changes via the GUI, be sure that the "Chip Address" has been set to '0'.

2. Set the "Register Address" to "0" to select the "ATTEN" register.
3. Select the desired attenuation step within the data field. Since the GRF640x series are 7-bit devices, there are 128 discrete 0.25 dB steps. Selecting a "0" in the data field places the DSA in its MINIMUM attenuation state. Conversely, selecting 127 will activate all of the attenuation cells, resulting in a MAXIMUM attenuation state of 31.75 dB. Use the following equation to select the desired attenuation state:

   ATTN State (decimal) = [ATTN State (dB)] / 0.25

4. Ensure that the PBAR/S box is SELECTED within the "Static Control" field prior to executing all serial commands. The "Parallel Control" fields can be ignored when simply programming the primary ATTEN DSA register.
5. Click on the "Serial Send" button to execute the SPI transaction. The DSA will load in the new attenuation value as soon as the SPI transaction is completed.

Utilizing the *Rapid Fire™* Feature Via the GUI

The control panel can be used to switch between the two attenuation states (standard and *Rapid Fire*) by simply using the PBAR/S checkbox in the "Static Control" field. However, in order to use the RFA feature, the *Rapid Fire* option must first be activated within the CONFIG register.

Enabling the *Rapid Fire* Feature on the GRF6403

1. Ensure that the PBAR/S box is *SELECTED* within the "Static Control" field.
2. Set the "Chip Address" to '0'.
3. Set the "Register Address" to 1 to select the CONFIG register.
4. Set the "Data" field to 2.
5. Hit the "Serial Send" button. Doing so will write a "10" to data bits D0-D1 within the CONFIG register.

Setting the *Rapid Fire* Attenuation State

Upon PORs (Power on Resets), the RFAREG (*Rapid Fire* register) will automatically be set to represent a full attenuation state of 31.75 dB. To override this default attenuation state, simply reprogram the values in RFAREG with the following steps:

1. Ensure that the PBAR/S box is *SELECTED* within the "Static Control" field.
2. Set the "Chip Address" to '0'.
3. Set the "Register Address" to 2 to select the RFAREG register.
4. Select the desired attenuation step within the data field. As with the ATTEN register, there are 128 discrete 0.25 dB steps that can be chosen. Selecting a "0" in the data field places the DSA in its MINIMUM attenuation state. Conversely, selecting 127 will activate all of the attenuation cells, resulting in a MAXIMUM attenuation state of 31.75 dB. Use the following equation to select the desired attenuation state:

   RFA ATTEN state (decimal) = [RFA ATTEN State (dB)] / 0.25

5. Hit the "Serial Send" button.

Alternatively, there is a mode where the GRF6403's external D0 - D6 pins can be used to set the logic for the *Rapid Fire* attenuation state. To use this approach, execute the following steps:

1. Ensure that the PBAR/S box is *SELECTED* within the "Static Control" field.
2. Set the "Chip Address" to '0'.
3. Set the "Register Address" to 1 to select the CONFIG register.
4. Set the "Data" field to 3. (Activates RFA feature AND instructs the pointer in bitfield [0] to use the logic on pins D0-D6 as the attenuation source.)
5. Hit the "Serial Send" button. Doing so will write a "11" to data bits D0-D1 within the CONFIG register.

6. Select the desired attenuation logic for pins D0 - D6 by *SELECTING/UNSELECTING* the respective boxes in the GUI's *Parallel Control* field.

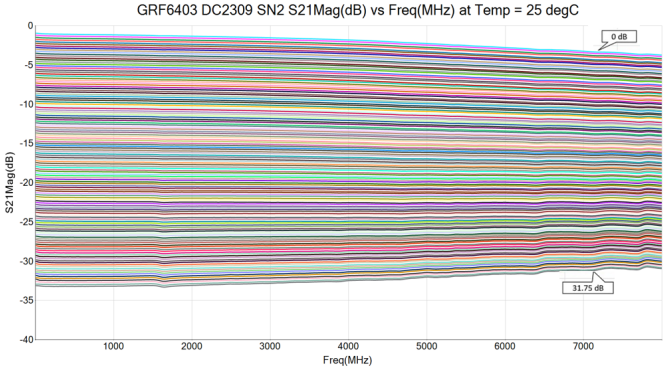
Toggling Between the Standard and *Rapid Fire* Attenuation States

Once the *Rapid Fire* feature has been enabled within the CONFIG register AND the desired Rapid Fire attenuation has been programmed in, simply *SELECT/UNSELECT* the PBAR/S box within the Static Control Field to toggle between the two different attenuation states.

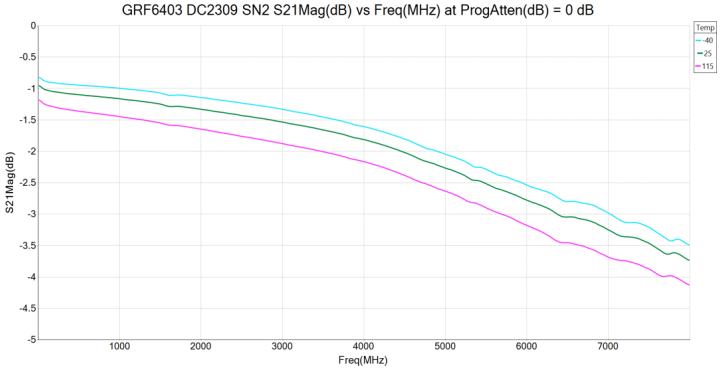
- PBAR/S box *UNSELECTED*: Logic LOW assigned to pin 3 [RFA Attenuation (from RFA Register 2 or external D0-D6 pin logic) Switched In]
- PBAR/S box *SELECTED*: Logic HIGH assigned to pin 3 [Primary Attenuation (from ATTEN Register 0) Switched In]

Please note that more in-depth programming details can be found in the "Detailed Register Map" section of this datasheet.

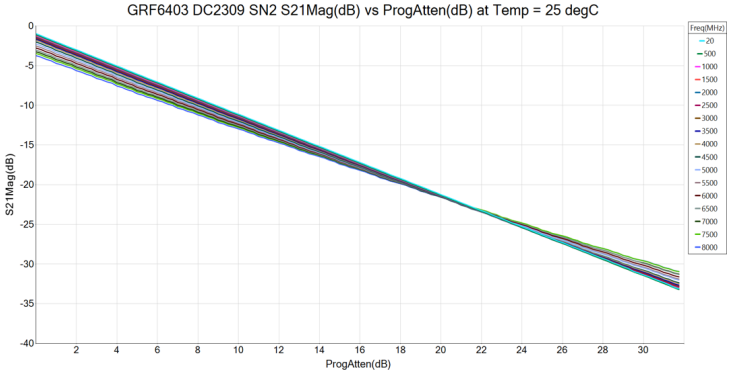
GRF6403 DC2309 SN2 S21Mag(dB) vs Freq(MHz) at Temp = 25 degC



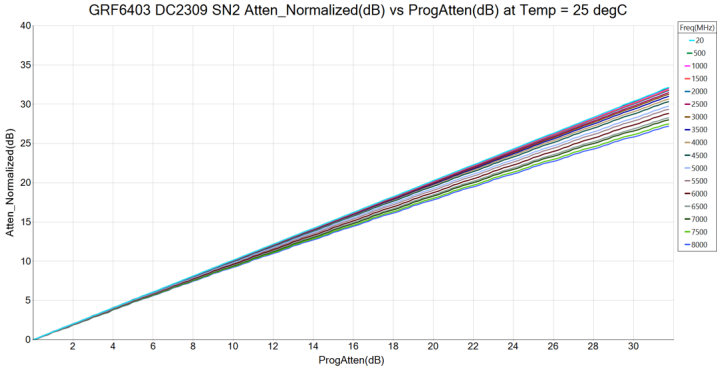
GRF6403 DC2309 SN2 S21Mag(dB) vs Freq(MHz) at ProgAtten(dB) = 0 dB



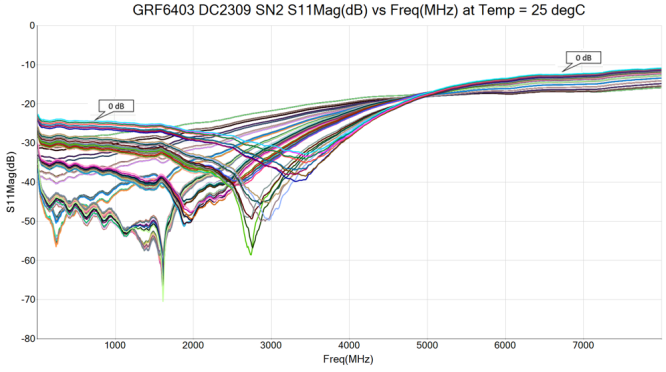
GRF6403 DC2309 SN2 S21Mag(dB) vs ProgAtten(dB) at Temp = 25 degC



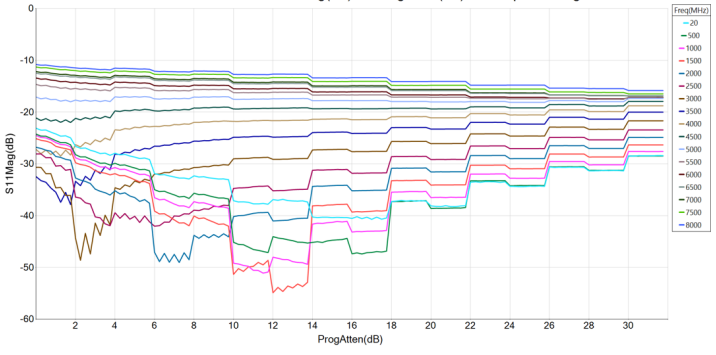
GRF6403 DC2309 SN2 Atten_Normalized(dB) vs ProgAtten(dB) at Temp = 25 degC



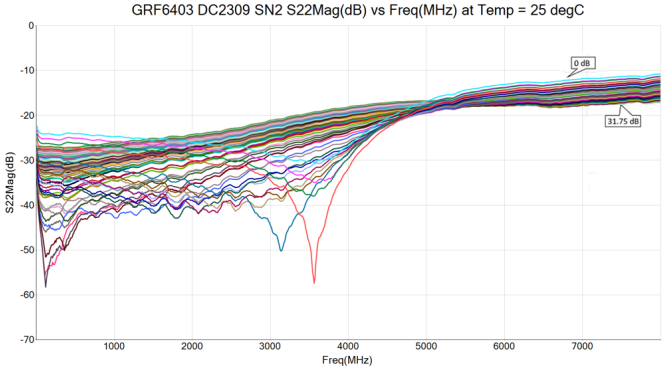
GRF6403 DC2309 SN2 S11Mag(dB) vs Freq(MHz) at Temp = 25 degC



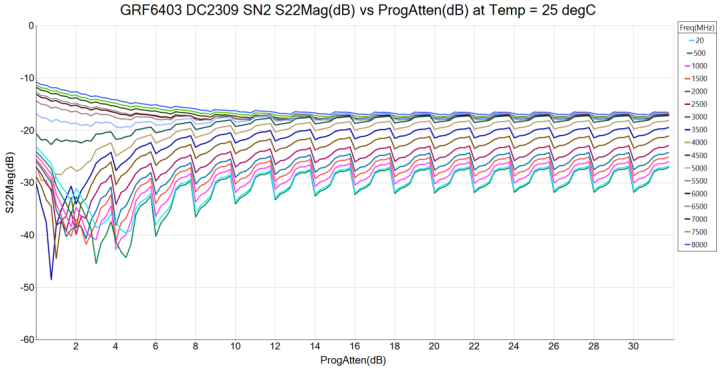
GRF6403 DC2309 SN2 S11Mag(dB) vs ProgAtten(dB) at Temp = 25 degC



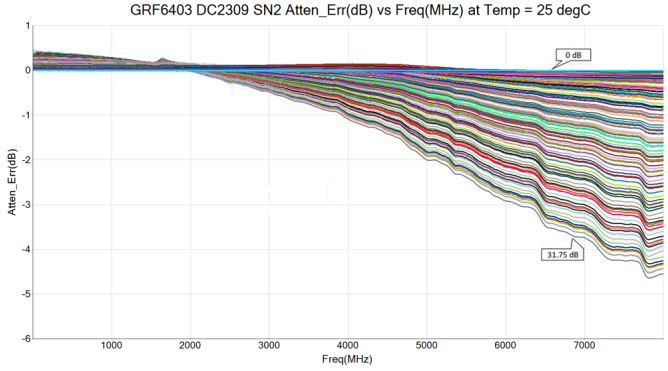
GRF6403 DC2309 SN2 S22Mag(dB) vs Freq(MHz) at Temp = 25 degC



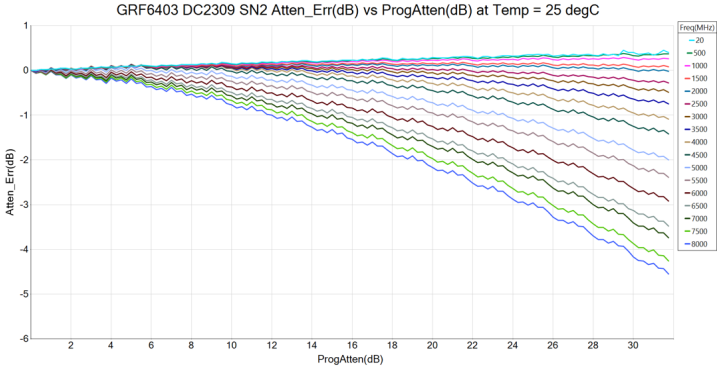
GRF6403 DC2309 SN2 S22Mag(dB) vs ProgAtten(dB) at Temp = 25 degC



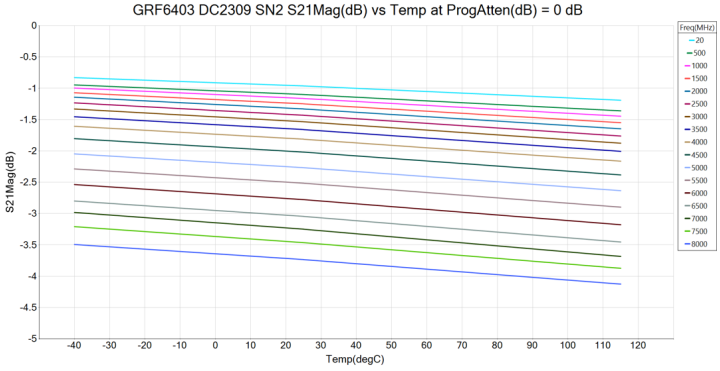
GRF6403 DC2309 SN2 Atten_Err(dB) vs Freq(MHz) at Temp = 25 degC



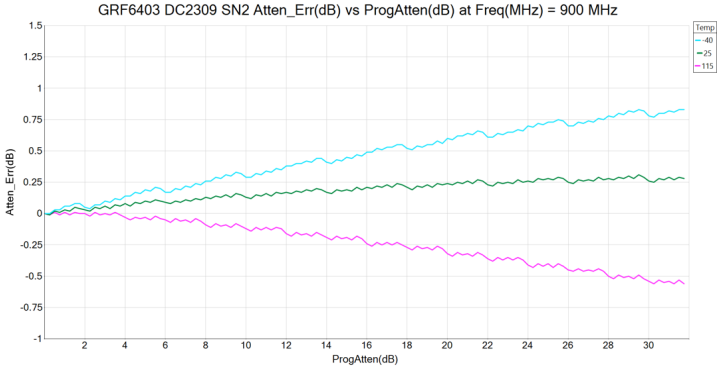
GRF6403 DC2309 SN2 Atten_Err(dB) vs ProgAtten(dB) at Temp = 25 degC

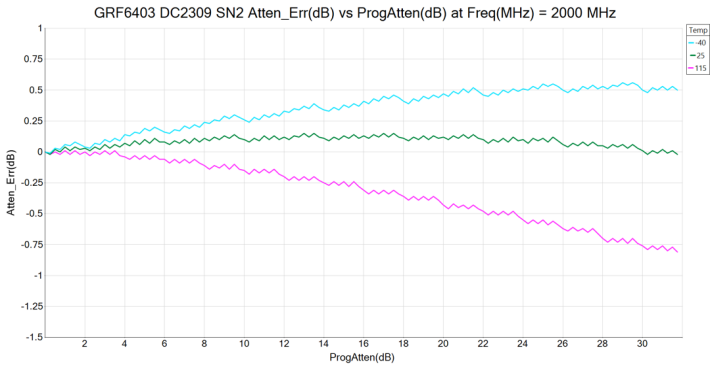


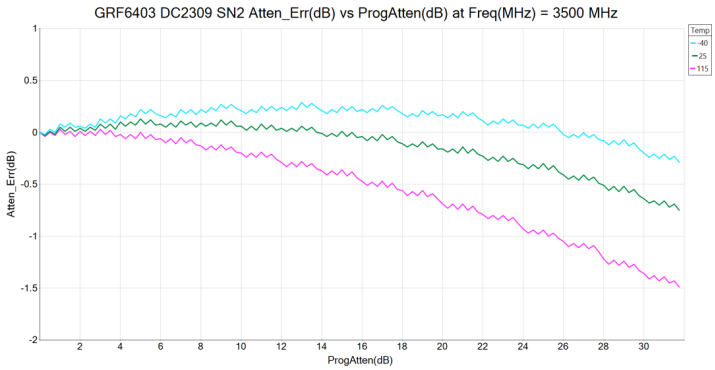
GRF6403 DC2309 SN2 S21Mag(dB) vs Temp at ProgAtten(dB) = 0 dB

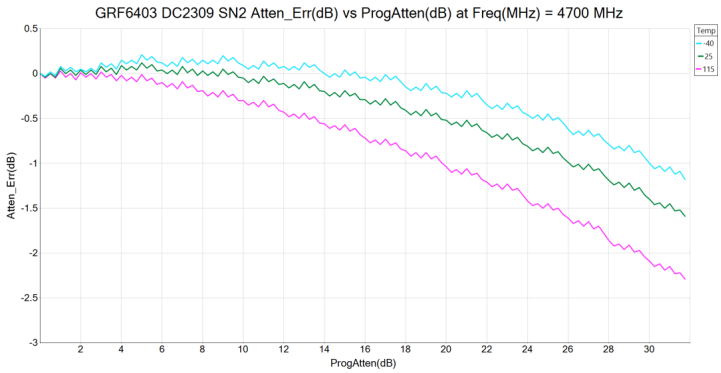


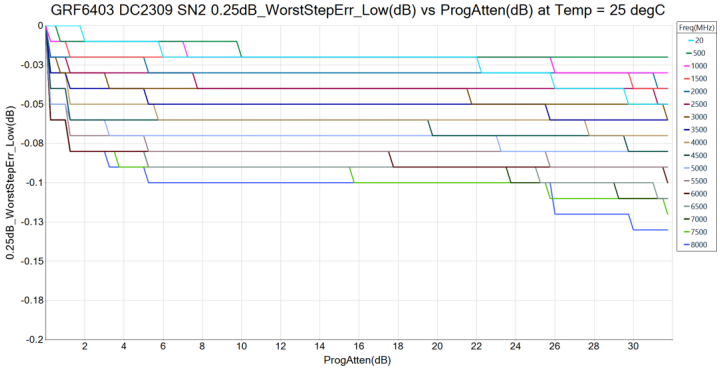
GRF6403 DC2309 SN2 Atten_Err(dB) vs ProgAtten(dB) at Freq(MHz) = 900 MHz

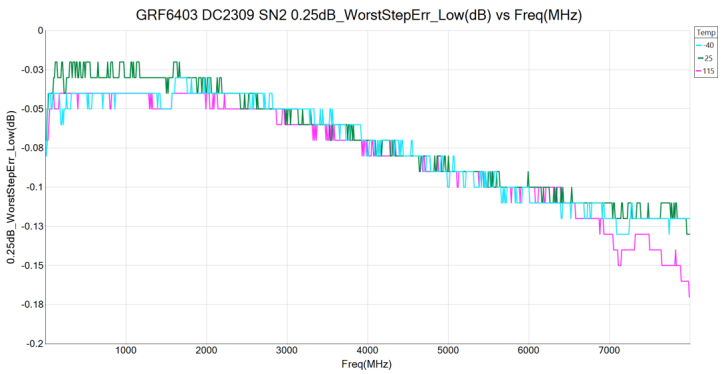


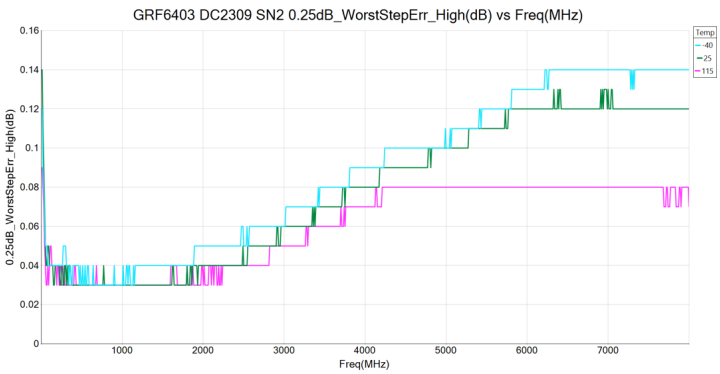


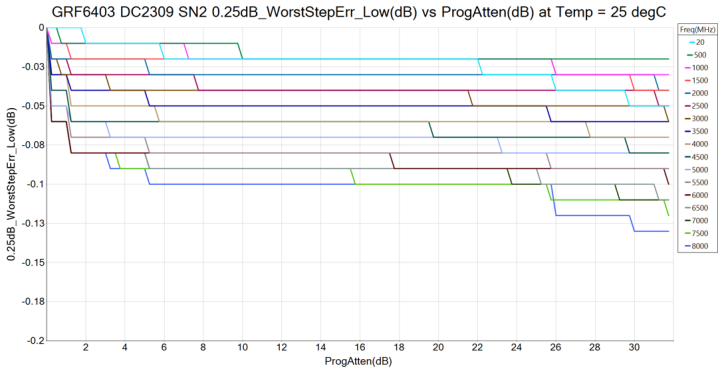


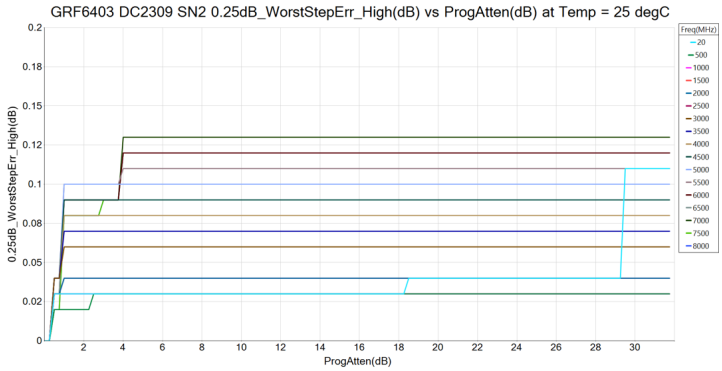


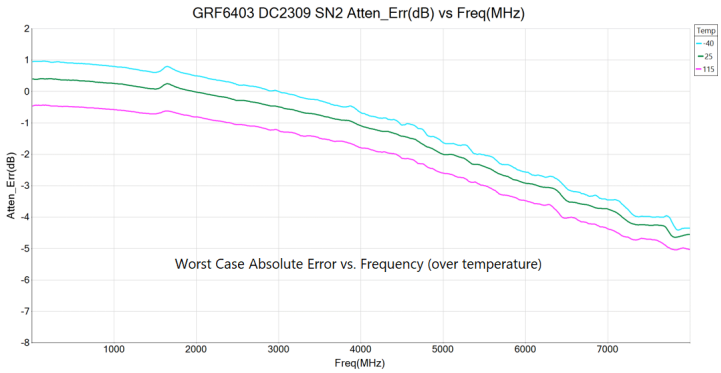


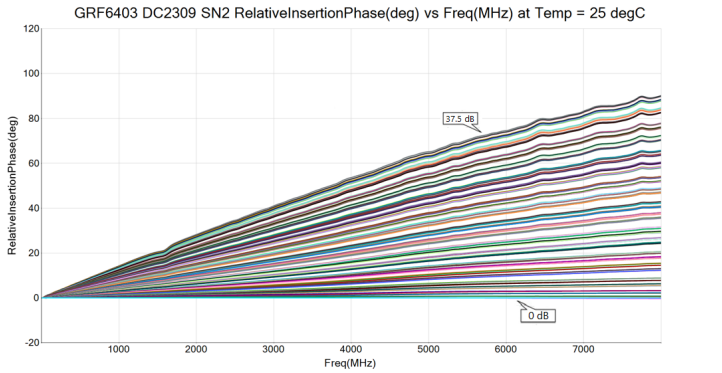


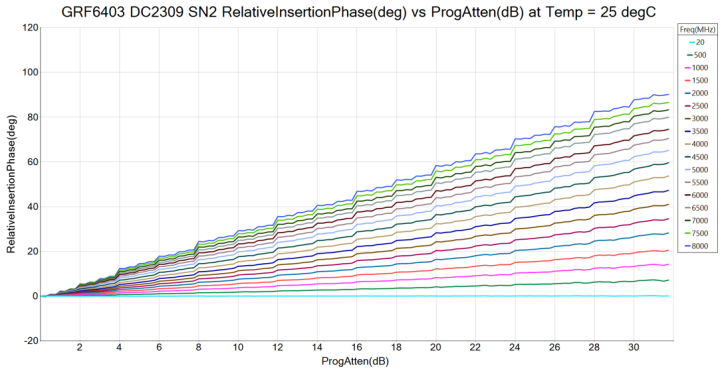


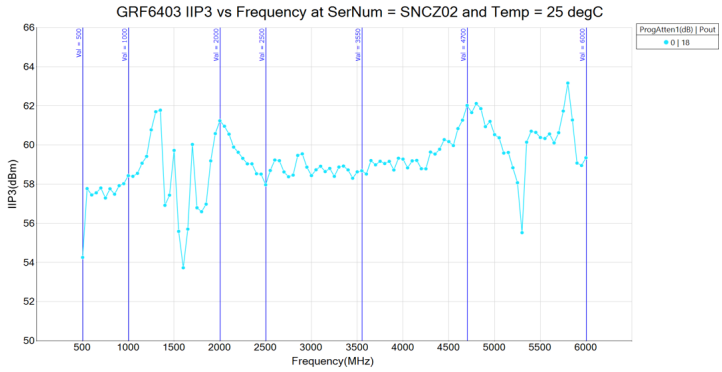




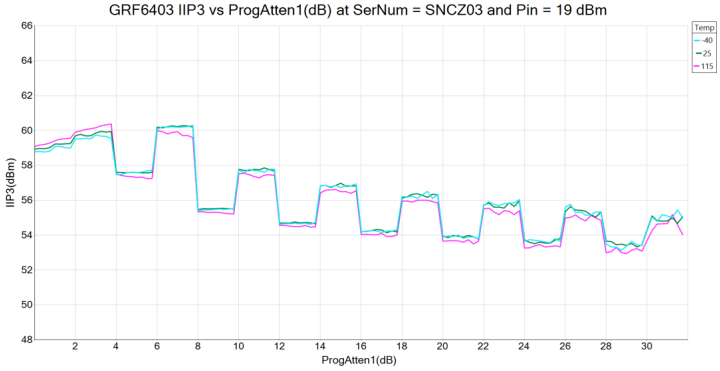




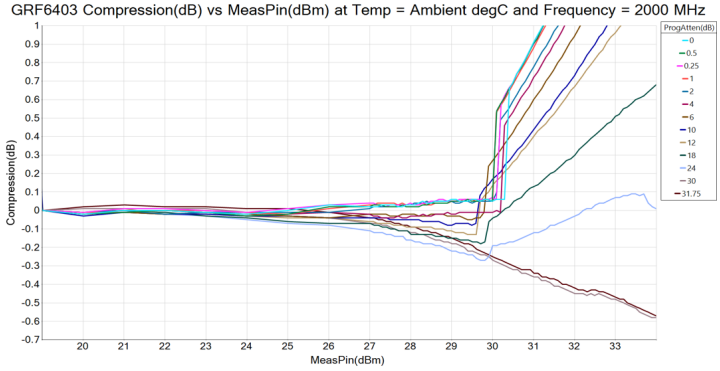




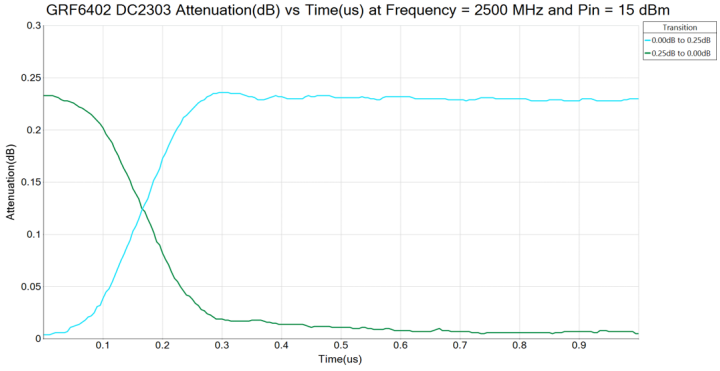
GRF6403 IIP3 vs ProgAtten1(dB) at SerNum = SNCZ03 and Pin = 19 dBm



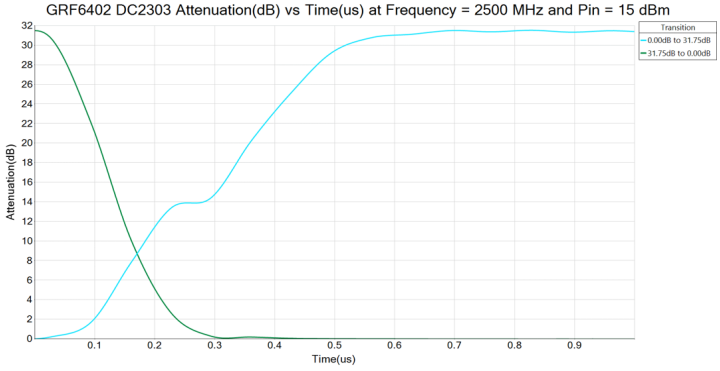
GRF6403 Compression(dB) vs MeasPin(dBm) at Temp = Ambient degC and Frequency = 2000 MHz



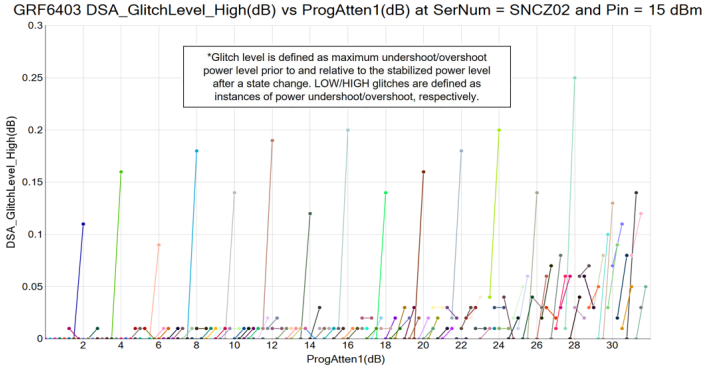
GRF6402 DC2303 Attenuation(dB) vs Time(us) at Frequency = 2500 MHz and Pin = 15 dBm



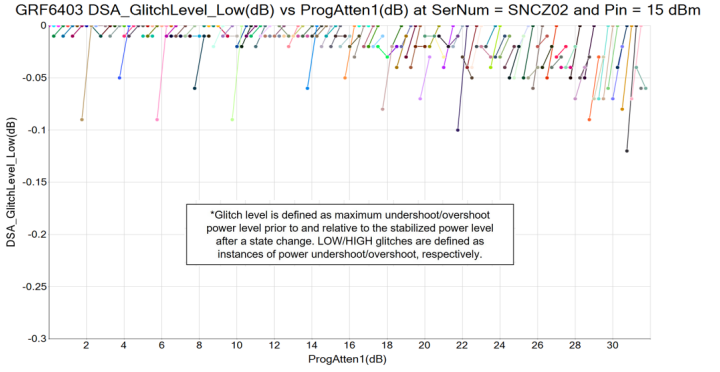
GRF6402 DC2303 Attenuation(dB) vs Time(us) at Frequency = 2500 MHz and Pin = 15 dBm



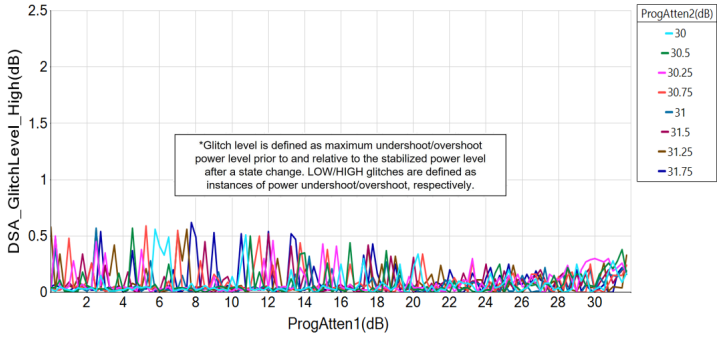
GRF6403 DSA_GlitchLevel_High(dB) vs ProgAtten1(dB) at SerNum = SNCZ02 and Pin = 15 dBm



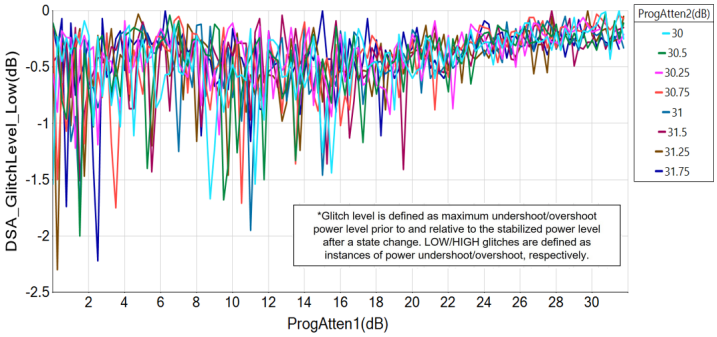
GRF6403 DSA_GlitchLevel_Low(dB) vs ProgAtten1(dB) at SerNum = SNCZ02 and Pin = 15 dBm

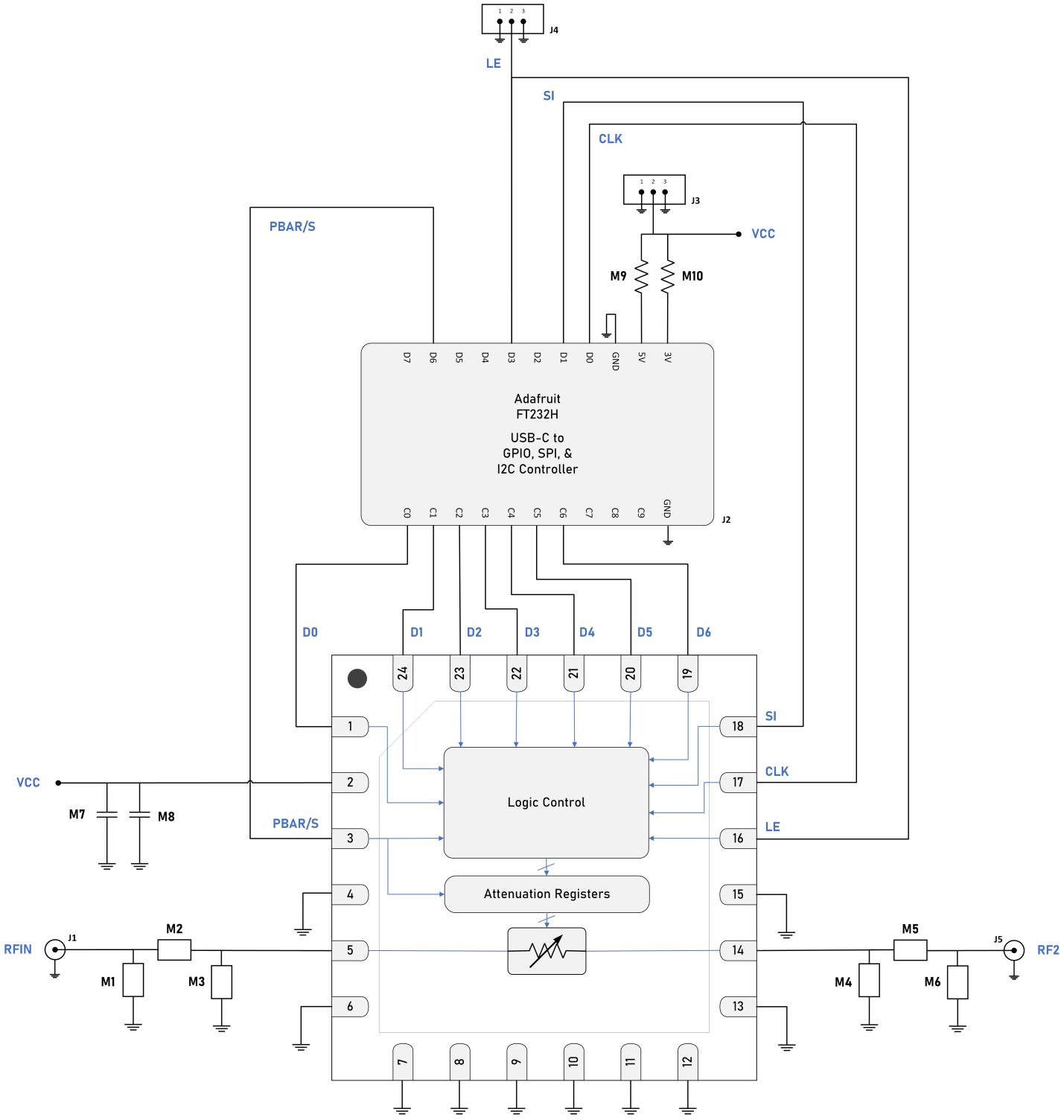


GRF6403 DSA_GlitchLevel_High(dB) vs ProgAtten1(dB) at Pin = 15 dBm



GRF6403 DSA_GlitchLevel_Low(dB) vs ProgAtten1(dB) at Pin = 15 dBm

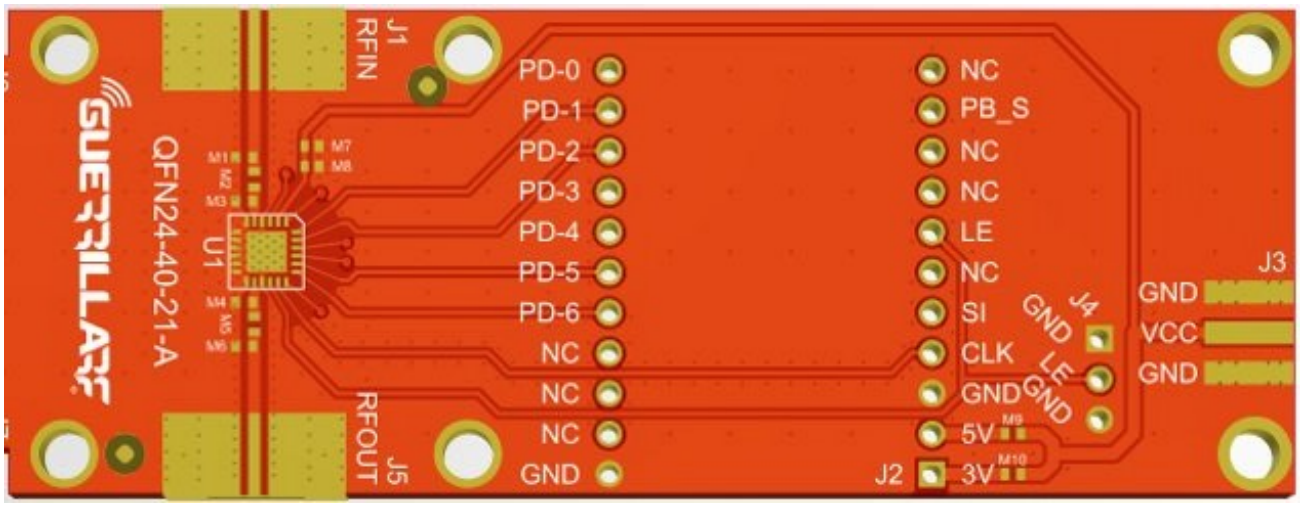




NOTE: *Do not apply DC voltage to pins 4 (RF1) and 9 (RF2).* DC blocking capacitors must be used if there is voltage present on the RF lines from the preceding or following stages. As a matter of good practice, it is recommended that DC blocks be used as a precaution.

The DSA will not generate DC voltages on either pins 1 and 9; as such, the blocking capacitors can be omitted in cases where it can be *guaranteed* that no DC will couple onto the RF lines from the preceding or following RF stages. Any DC voltage applied to the RF1 and RF2 pins may lead to electrical overstress, so be cautious when contemplating the removal of these components.

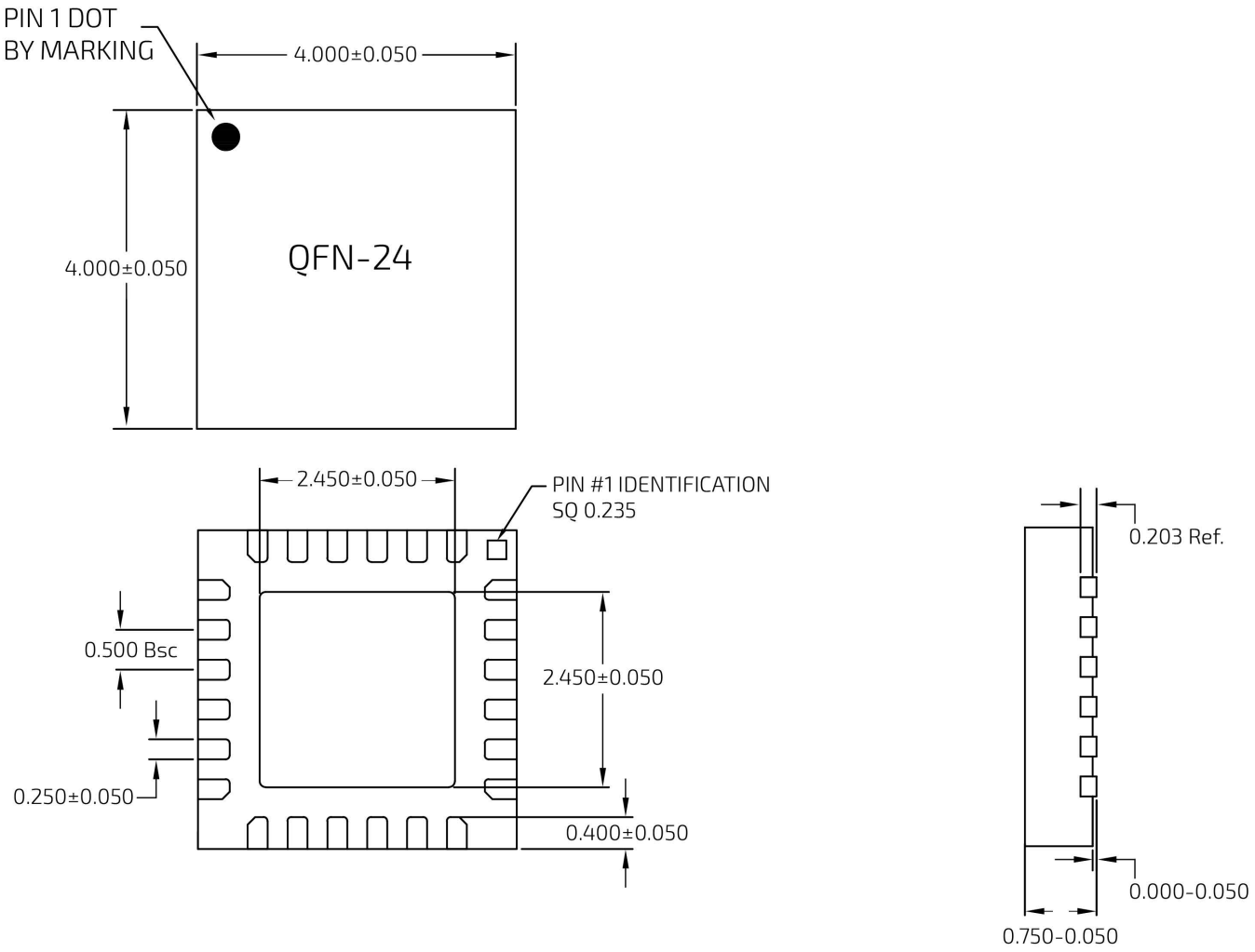
GRF6403 Application Schematic



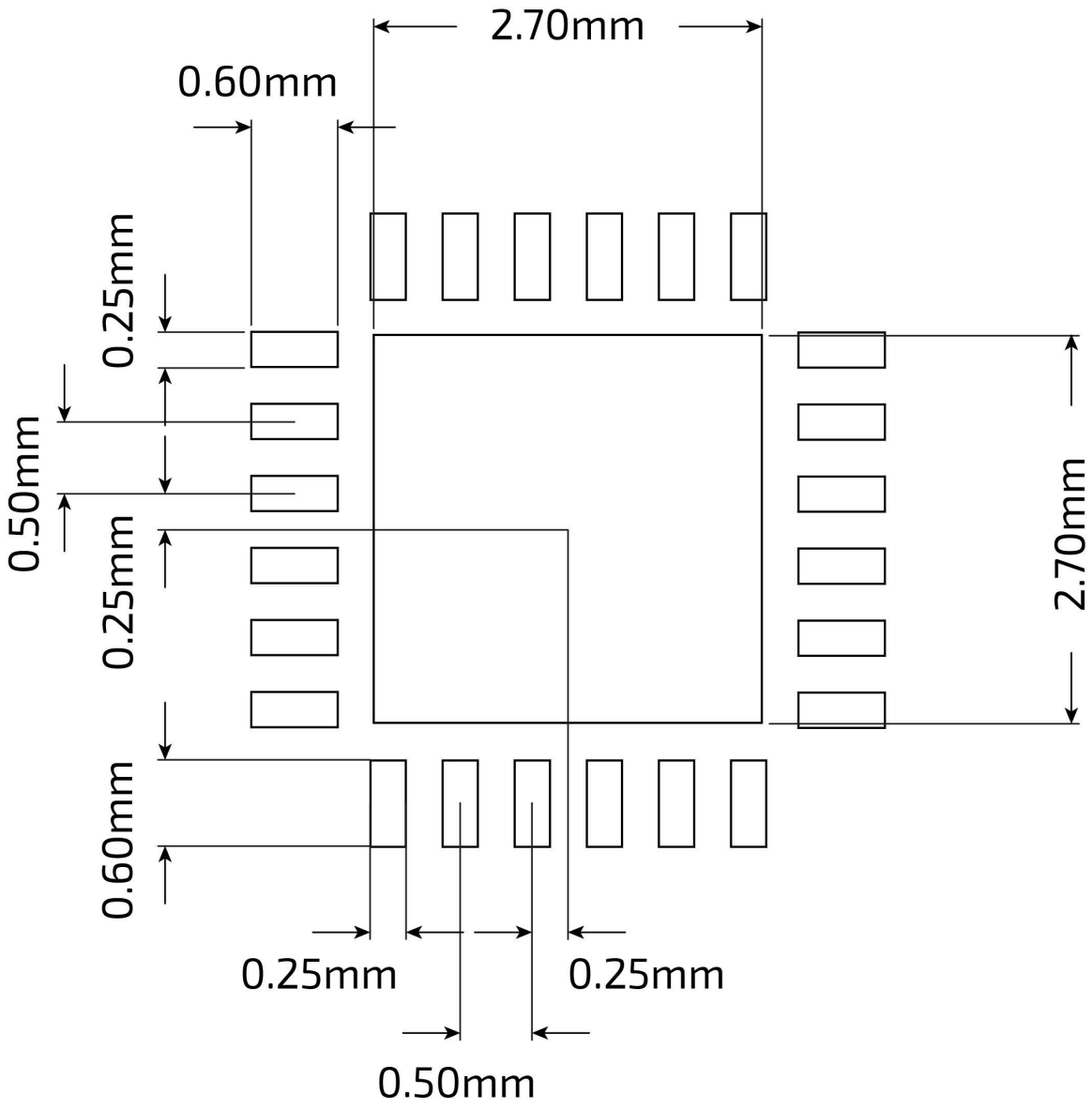
GRF6403 Evaluation Board Assembly Diagram

GRF6403 Evaluation Board Assembly Diagram Reference

Component	Type	Manufacturer	Family	Value	Package Size	Substitution
M1	--	--	--	--	--	--
M2	Jumper, Solid Copper	Koa/Speer	TLRZ1ETTB	0 Ω	0402	Ok
M3	--	--	--	--	DNP	--
M4	--	--	--	--	DNP	--
M5	Jumper, Solid Copper	Koa/Speer	TLRZ1ETTB	0 Ω	0402	--
M6	--	--	--	--	DNP	--
M7	Capacitor	Murata	GRM	10 nF	0402	Ok
M8	Capacitor	Murata	GRM	1 µF	0402	Ok
J1	RF Jack, 10 GHz	Johnson	SMA	147-0701-851	--	Ok
J5	RF Jack, 10 GHz	Johnson	SMA	147-0701-851	--	Ok
Control Board	F232H USB-C to GPIO, SPI and I2C Controller	Adafruit	--	--	--	--
Evaluation Board	QFN24-40-21-A	--	--	--	--	--



QFN 24 4x4mm Package Dimensions



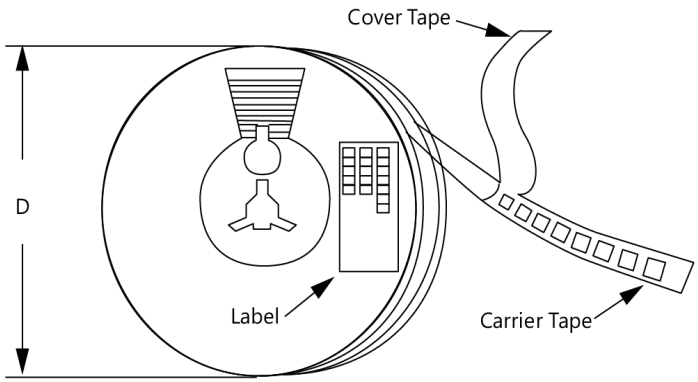
QFN 24 4x4mm Suggested PCB Footprint (Top View)

Package Marking Diagram

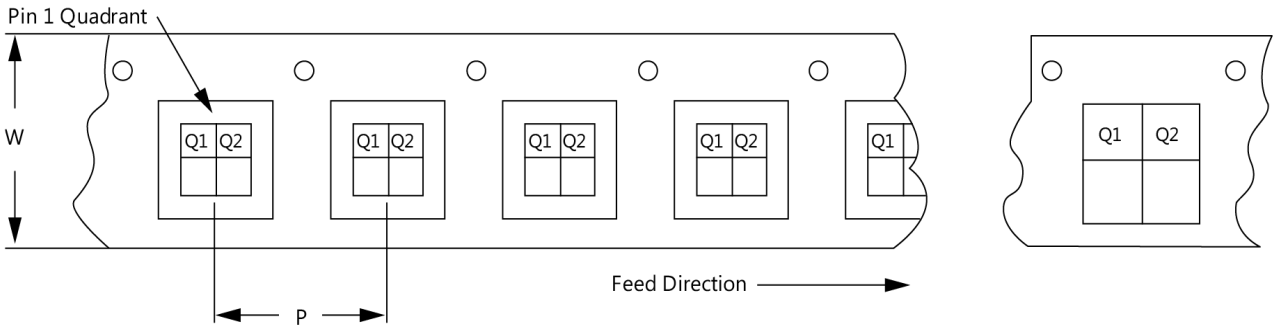
Line 1: "YY" = Year. "WW" = WORK WEEK the Device was assembled.
Line 2: "GRF" = Guerrilla RF.
Line 3: "XXXX" = Device Part Number.

Tape and Reel Information

Guerrilla RF's tape and reel specification complies with Electronics Industries Association (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag, and the outside surface of the box. For the latest reel specifications and package information (including units/reel), please visit Package Manufacturing Information | Guerrilla RF (guerrilla-rf.com).



Tape and Reel Packaging with Reel Diameter Noted (D)



Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information

Revision History

Revision Date	Description of Change
7/28/2023	Advance Datasheet - First Draft
1/25/2024	Advance Datasheet - Increased CDM ESD limit from 500 V to 750 V. Updated applications schematic to include Adafruit FT232H USB-C to GPIO, SPI and I2C Controller. Revised programming section to properly define the *Rapid Fire* Pointer Flag within the CONFIG register. With this corrected setting, a '0' assigned to bit [0] in the CONFIG register pulls the *Rapid Fire* attenuation value directly from the RFAREG register. Updated the GUI programming section.
2/23/2024	Updated the thermal resistance and junction temperature values within the 'nominal operating parameters' table.
August 21, 2024	Release Ø Data Sheet. Upgraded data sheet to new format. Updated the specifications in the nominal operating parameters' table. Updated plots on pages 29-34.
November 21 2024	Added verbiage to LE pin description clarifying that data is latched into the registers when the LE pin transitions from LOW to HIGH and then back to LOW. Replaced package drawings with corrected versions (which pertain to the 4x4 QFN-24 package type). Added new Glitch-Level High & Low plots.
February 21, 2025	Updated PCB footprint.

Data Sheet Classifications

Data Sheet Status	Notes
Advance	S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices.
Preliminary	All data based on evaluation board measurements taken within the Guerrilla RF Applications Lab. Any MIN/MAX limits represented within the data sheet are based solely on *estimated* part-to-part variations and process spreads. All parametric values are subject to change pending the collection of additional data.
Release Ø	All data based on measurements taken with *production-released* material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory.
Release A-Z	All data based on measurements taken with production-released material *derived from multiple lots which have been fabricated over an extended period of time*. MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads.