

Specification

Part No.: DLC70B

DLC70B (.110" x .110")



◆ Product Features

High Q, High Power, Low ESR/ESL, Low Noise,
High Self-Resonance, Ultra-Stable Performance.

◆ Product Application

Typical Functional Applications: Bypass, Coupling, Tuning, Feedback, Impedance Matching and D.C. Blocking.

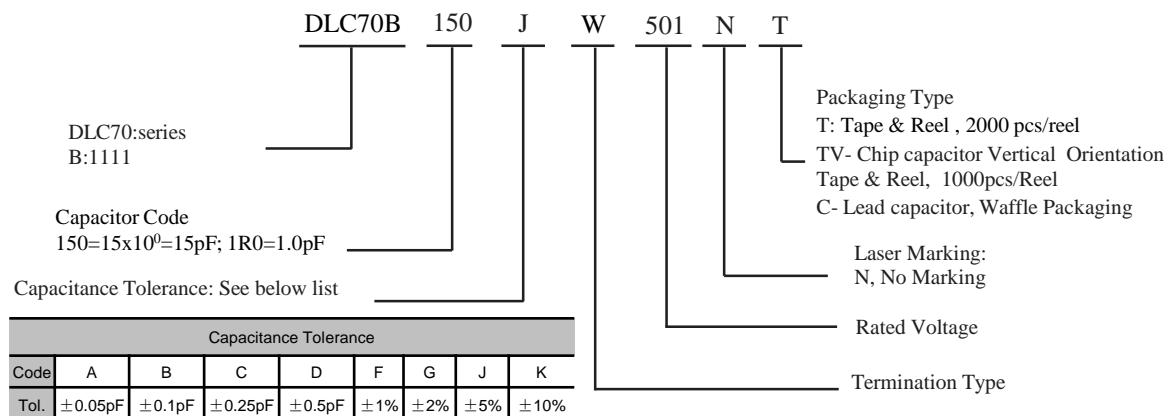
Typical Circuit Applications: UHF/Microwave RF Power Amplifiers, Mixers, Oscillators, Low Noise Amplifiers, Filter Networks, Timing Circuits and Delay Lines.

◆ DLC70B Capacitance Table

Cap. pF	Code	Tol.	Rated WVDC	Cap. pF	Code	Tol.	Rated WVDC	Cap. pF	Code	Tol.	Rated WVDC	Cap. pF	Code	Tol.	Rated WVDC	
0.1	0R1	A,B	500V Code 501 or 1500V Code 152	3.6	3R6	A,B, C,D	500V Code 501 or 1500V Code 152	43	430	F,G, J	500V Code 501 or 1500V Code 152	510	511	F,G, J	100V Code 101 or 300V Code 301	
0.2	0R2			3.9	3R9			47	470			560	561			
0.3	0R3			4.3	4R3			51	510			620	621			
0.4	0R4			4.7	4R7			56	560			680	681			
0.5	0R5			5.1	5R1			62	620			750	751			
0.6	0R6			5.6	5R6			68	680			820	821			
0.7	0R7			6.2	6R2			75	750			910	911			
0.8	0R8			6.8	6R8			82	820			1000	102			
0.9	0R9			7.5	7R5			91	910			1100	112	G,J	300V Code 301	
1.0	1R0			8.2	8R2			100	101			1200	122			
1.1	1R1			9.1	9R1			110	111			1500	152			
1.2	1R2			10	100			120	121			1800	182			
1.3	1R3	A,B, C,D		11	110			130	131	F,G, J	300V Code 301 or 1000V Code 102	2200	222	G,J	100V Code 101 or 200V Code 201	
1.4	1R4			12	120			150	151			2700	272			
1.5	1R5			13	130			160	161			3000	302			
1.6	1R6			15	150			180	181			3300	332			
1.7	1R7			16	160			200	201			3900	392			
1.8	1R8			18	180			220	221			4700	472			
1.9	1R9			20	200			240	241			5100	512			
2.0	2R0			22	220			270	271			5600	562			
2.1	2R1			24	240			300	301			10000	103			
2.2	2R2			27	270			330	331							
2.4	2R4			30	300			360	361							
2.7	2R7			33	330			390	391							
3.0	3R0			36	360			430	431							
3.3	3R3			39	390			470	471							

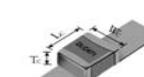
Remark: special capacitance, tolerance and WVDC are available, consult with DALICAP.

◆ Part Numbering

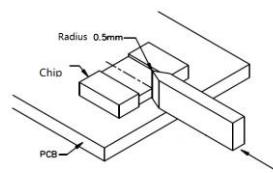


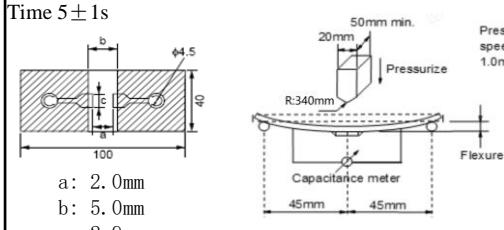
◆ DLC70B Termination Type and Dimensions

unit: inch (millimeter)

Series	Term. Code	Type/ Outlines	Capacitor Dimensions				Lead Dimensions			Plated Material
			Length L _c	Width W _c	Thickness T _c	Overlap B	Length L _L	Width W _L	Thickness T _L	
70B	W	 Chip	.110	.110±.010	.100	.016~.039 (0.40~1.00)	—	—	—	100%Sn over Nickel Plating, RoHS Compliant
	L		-.010~+.025 (2.79~0.63)	(2.79±0.25)	(2.54)max	—	—	—	—	90%Sn 10%Pb over Nickel Plating,
70B	MS	 Microstrip	.110	.110±.010	.100	—	.250 (6.35)min	.093±.010 (2.36±0.25)	.004±.001 (0.1±.025)	100% silver.
Series	Term. Code	Type/ Outlines	Capacitor Dimensions				Lead Dimensions			Plated Material
			Length L _c	Width W _c	Thickness T _c	Overlap B	Length L _L	Width W _L	Thickness T _L	
70B	P	 Chip(Non-Mag)	.110	.110±.010	.100	.016~.039 (0.40~1.00)	—	—	—	100%Sn over Copper Plating, RoHS Compliant
70B	MN	 Microstrip(Non-Mag)	.110	.110±.010	.100	—	.250 (6.35)min	.093±.010 (2.36±0.25)	.004±.001 (0.1±.025)	100% silver.

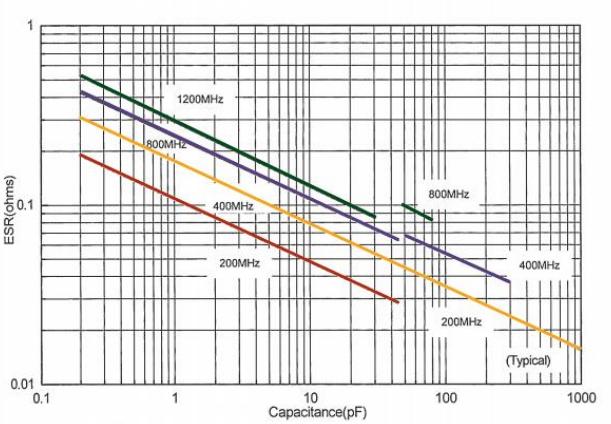
◆ Reliability Test Conditions.

No.	Item	Specification	Test method												
1	Operating temperature	-55°C~125°C	-												
2	Appearance	No defects or abnormality	Visual inspection: × 10 microscope.												
3	Dimensions	See the previous page	Caliper inspection												
4	Capacitance	Shall be within the applicable tolerance specified.	Test frequency: C≤1000pF: 1MHz±10% C>1000pF: 1KHz±10%												
5	D.F	C≤1.5pF: DF≤0.10% 1.5 pF<C<100pF: DF≤0.05% C≥100pF: DF≤0.10%	Test voltage: 1.0±0.2Vrms												
6	Insulation resistance	10 ⁵ Megohms min. @ +25 °C 10 ⁴ Megohms min. @ +125 °C	Voltage: DC Rated Voltage (500V max)												
7	Dielectric withstanding voltage (DWV)	Shall be no evidence of breakdown or visible evidence of arcing or damage.	Test Voltage: Rated voltage≤500V: 250% of the rated voltage 500V<Rated voltage≤1250V: 150% of the rated voltage Rated voltage>1250V: 120% of the rated voltage Applied Time: 1s to 5 s Charge/discharge current: 50mA max.												
8	Temperature coefficient	(0±30)ppm/°C	The capacitance change should be measured after 5 min. at each specified temp. stage. Capacitance value as a reference is the value in step 3. <table border="1" data-bbox="756 1180 1101 1430"> <tr> <th>step</th><th>temperature (°C)</th></tr> <tr> <td>1</td><td>25±2</td></tr> <tr> <td>2</td><td>-55±3</td></tr> <tr> <td>3</td><td>25±2</td></tr> <tr> <td>4</td><td>125±3</td></tr> <tr> <td>5</td><td>25±2</td></tr> </table> $TC = \frac{C_x - C_3}{C_3 \times \Delta T} \times 10^6 \text{ ppm/}^{\circ}\text{C}$	step	temperature (°C)	1	25±2	2	-55±3	3	25±2	4	125±3	5	25±2
step	temperature (°C)														
1	25±2														
2	-55±3														
3	25±2														
4	125±3														
5	25±2														
9	Adhesive Strength of Termination	No removal of the terminations or other defect should occur.	Pressurizing force: 22.0 ^{+1.0} ₀ N Test time: 10±1 sec. 												

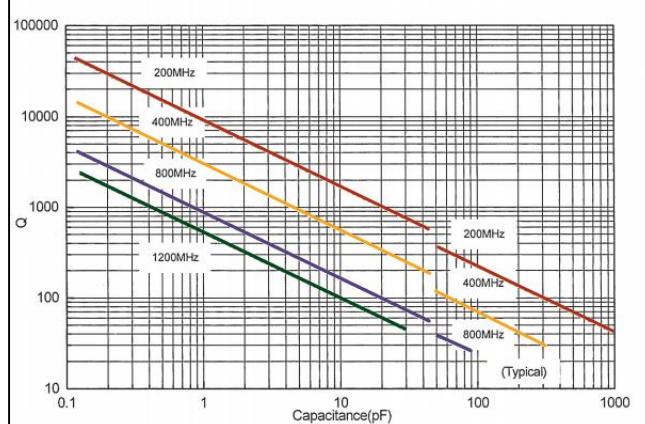
No.	Item	Specification	Test method															
10	Substrate Bending test	Appearance: No defects or abnormalities. Capacitance Change: Within $\pm 5\%$ or $\pm 0.3\text{pF}$ whichever is larger.	Mounting method: Reflow solder the capacitor on the test substrate. Pressurization Method: Shown as below. Flexure 1mm. Holding Time 5 ± 1 s 															
11	Solderability of termination	Shall be at least 95 percent covered with a smooth solder coating.	Immerse the capacitor in a eutectic solution requirement temperature $245 \pm 2^\circ\text{C}$ for 2 ± 0.5 seconds. Capacitor shall be immersed to a depth of 10mm.															
12	Resistance to soldering Heat	Appearance: No evidence of mechanical damage or delamination or exposed. Cap change: within $-1.0\% \sim +2.0\%$ or $\pm 0.5\text{pF}$ whichever is larger. Q: To meet initial requirement. IR(25°C): To meet initial requirement.	Immerse the capacitor in a eutectic solution at $260 \pm 5^\circ\text{C}$ for 10 ± 1 seconds. Capacitor shall be immersed to a depth of 10mm. And following a 24 ± 2 hours cooling period.															
13	Temperature Cycle	Appearance: No evidence of mechanical damage . Cap change: within $\pm 0.5\%$ or $\pm 0.5\text{pF}$ whichever is larger. Q: To meet initial requirement. IR(25°C): No less than 30% initial requirement. DWV: To meet initial requirement.	Perform the 5 cycles according to the four heat treatments listed in the following table. Set it for 24 ± 2 hours at room temperature. <table border="1" data-bbox="770 1123 1202 1305"> <thead> <tr> <th>step</th><th>Temperature($^\circ\text{C}$)</th><th>Time(min)</th></tr> </thead> <tbody> <tr> <td>1</td><td>-55(-3~0)</td><td>≥ 30</td></tr> <tr> <td>2</td><td>25+10</td><td>≤ 5</td></tr> <tr> <td>3</td><td>125(0~+3)</td><td>≥ 30</td></tr> <tr> <td>4</td><td>25+10</td><td>≤ 5</td></tr> </tbody> </table>	step	Temperature($^\circ\text{C}$)	Time(min)	1	-55(-3~0)	≥ 30	2	25+10	≤ 5	3	125(0~+3)	≥ 30	4	25+10	≤ 5
step	Temperature($^\circ\text{C}$)	Time(min)																
1	-55(-3~0)	≥ 30																
2	25+10	≤ 5																
3	125(0~+3)	≥ 30																
4	25+10	≤ 5																
14	Humidity, steady state	Appearance: No evidence of mechanical damage . Cap change: within $\pm 0.3\%$ or $\pm 0.3\text{pF}$ whichever is larger. IR(25°C): No less than 10% initial requirement.	With (1.3 ± 0.25) Volts D.C. applied while subjected to an environment of 85°C with 85% relative humidity for 240 hours minimum. Removed and sit 3.5 ± 0.5 hours at room temperature.															
15	High Temperature Load (Life)	Appearance: No evidence of mechanical damage . Cap change: within $\pm 2\%$ or $\pm 0.5\text{pF}$ whichever is larger. IR(25°C): No less than 30% initial requirement. Q: > 1000 .	Test Voltage: Rated voltage $\leq 500\text{V}$: 200% of the rated voltage $500\text{V} < \text{Rated voltage} \leq 1250\text{V}$: 120% of the rated voltage $\text{Rated voltage} > 1250\text{V}$: 100% of the rated voltage The charge/discharge current is less than 50mA. Temperature: 125°C ; Time: 2000h. Measurement: Set it for 48 hours at room temperature, then measure.															

◆ **DLC70B Performance Curve**

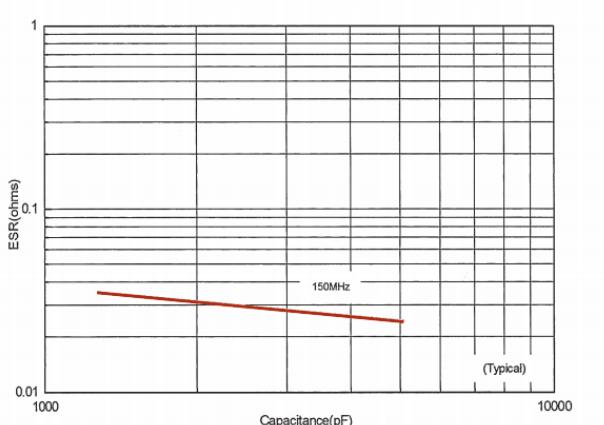
ESR vs Capacitance



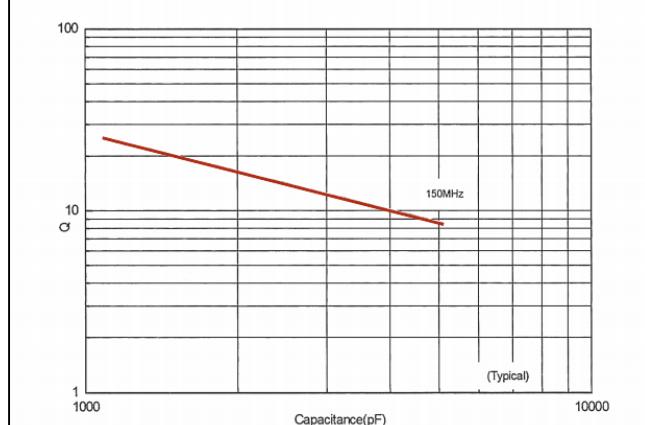
Q vs Capacitance



ESR vs Capacitance

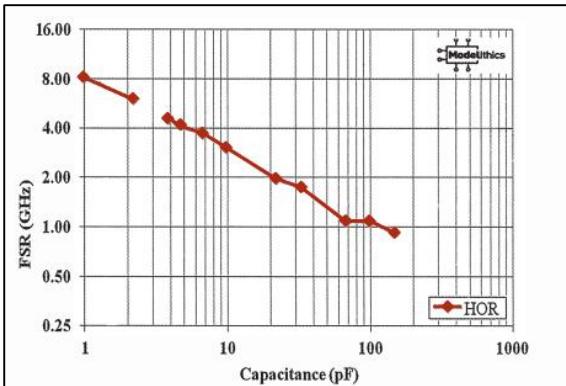


Q vs Capacitance

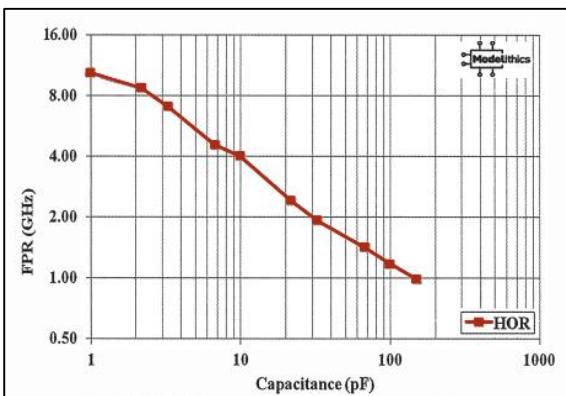


◆ DLC70B Performance Curve

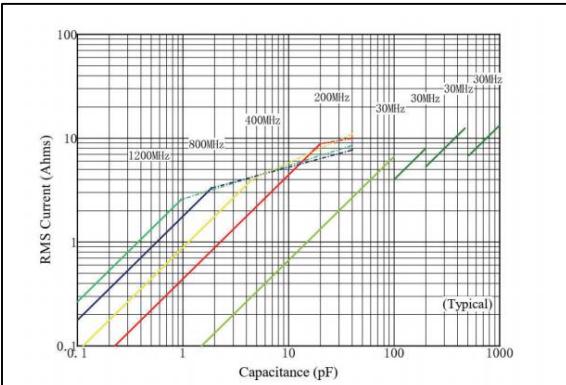
Horizontal First Series Resonance (FSR)



Horizontal First Parallel Resonance (FPR)



RMS Current vs Capacitance



Definitions and Measurement Conditions

For a capacitor in a series configuration, i.e., mounted across a gap in a microstrip trace, with 50-Ohm source and termination resistances, the First Series Resonance, FSR, is defined as the lowest frequency at which the imaginary part of the input impedance, $\text{Im}[\text{Zin}]$, equals zero. Should $\text{Im}[\text{Zin}]$ or the real part of the input impedance, $\text{Re}[\text{Zin}]$, not be monotonic with frequency at frequencies lower than those at which $\text{Im}[\text{Zin}] = 0$, the FSR shall be considered as undefined (gap in plot above). FSR is dependent on internal capacitor structure; substrate thickness and dielectric constant; capacitor orientation, as defined above; and mounting pad dimensions.

The measurement conditions are: substrate -- Rogers RO4350; substrate dielectric constant = 3.66; horizontal mount substrate thickness (mils) = 50; gap in microstrip trace (mils) = 72; horizontal mount microstrip trace width (mils) = 110.

Reference planes at sample edges.

All data has been derived from electrical models created by Modelithics, Inc., a specialty vendor contracted by DLC. The models are derived from measurements on a large number of parts disposed on several different substrates.

Definitions and Measurement conditions:

For a capacitor in a series configuration, i.e., mounted across a gap in a microstrip trace, with 50-Ohm source and termination resistances, the First Parallel Resonance, FPR, is defined as the lowest frequency at which a suckout or notch appears in $|\text{S21}|$. It is generally independent of substrate thickness or dielectric constant, but does depend on capacitor orientation. A horizontal orientation means the capacitor electrode planes are parallel to the plane of the substrate; a vertical orientation means the electrode planes are perpendicular to the substrate. The measurement conditions are: substrate -- Rogers RO4350; substrate dielectric constant = 3.66; horizontal mount substrate thickness (mils) = 50; gap in microstrip trace (mils) = 72; horizontal mount microstrip trace width (mils) = 110.

Reference planes at sample edges.

All data has been derived from electrical models created by Modelithics, Inc., a specialty vendor contracted by DLC. The models are derived from measurements on a large number of parts disposed on several different substrates.

The current depends on voltage limited:

$$I = \frac{\sqrt{2}}{2} I_{\text{peak}} = \frac{\sqrt{2}}{2} \times \frac{V_{\text{rated}}}{X_C} = \sqrt{2\pi f C V_{\text{rated}}}$$

The current depends on power dissipation limited:

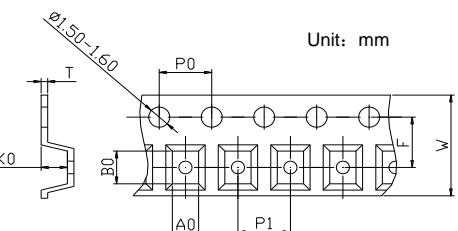
$$I = \sqrt{\frac{P_{\text{dissipation}}}{ESR}}$$

The current rating is based on a 65°C mounting surface and a device thermal resistance of 20°C/W. A Power dissipation of 3W

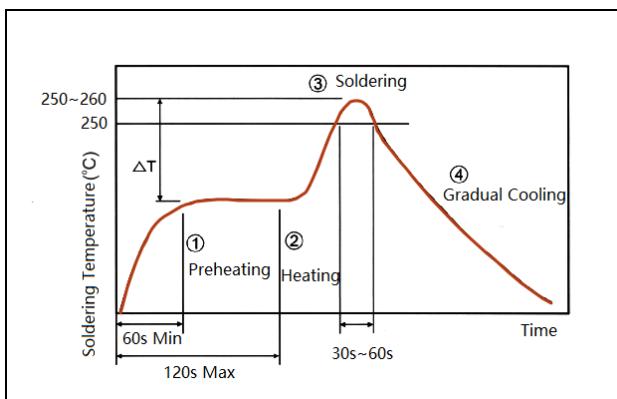
$$I = \sqrt{\frac{P_{\text{dissipation}}}{ESR}}$$

◆ Tape & Reel Specifications

Orientation	EIA	A0	B0	K0	W	P0	P1	T	F	Qty/reel	Tape Material
Horizontal	1111	2.85	3.50	1.95	8.00	4.00	4.00	0.25	3.50	2000	Plastic
Horizontal	1111	2.85	3.60	2.40	8.00	4.00	4.00	0.25	3.50	2000	Plastic
Vertical	1111	2.30	3.55	2.70	12.00	4.00	4.00	0.40	5.50	1500	Plastic



◆ Recommended soldering conditions



$\Delta T \leq 190^\circ\text{C}$;

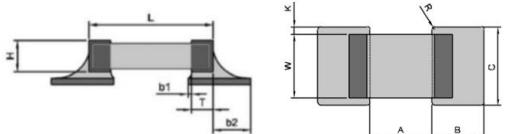
Maximum temperature: $255^\circ\text{C} \pm 5^\circ\text{C}$;

Heating rate: $\leq 4^\circ\text{C/s}$.

◆ Recommended Land Dimensions

Horizontal Mounting

Orientation	EIA	A(mm)	B(mm)	C(mm)
Horizontal	1111	2.0	1.5	2.8



Vertical Mounting

Orientation	EIA	A(mm)	B(mm)	C(mm)
Vertical	1111	1.9	1.7	2.5

