

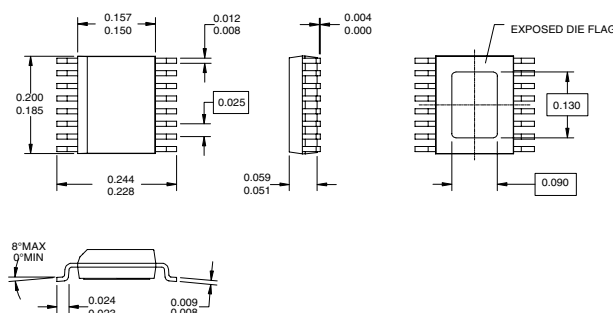
PCS CDMA LOW NOISE AMPLIFIER/MIXER 1500MHZ TO 2200MHZ DOWNCONVERTER

Typical Applications

- CDMA PCS Handsets
- TDMA PCS Handsets
- GSM PCS Handsets
- General Purpose Receiver Front-End
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

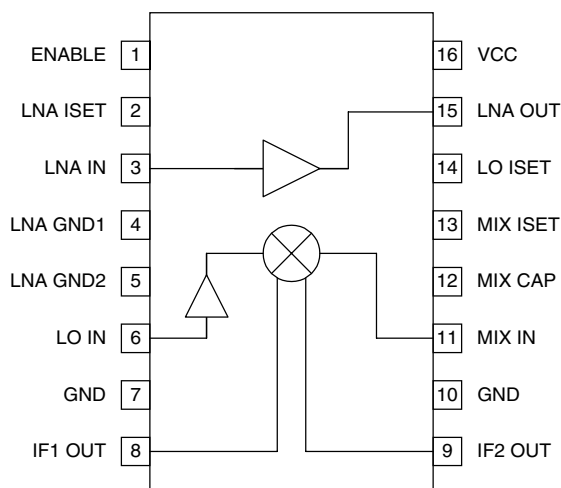
Product Description

The RF2448 is a receiver front-end designed for the receive section of PCS CDMA, TDMA and GSM applications. It is designed to amplify and downconvert RF signals. A further feature of the chip is adjustable IIP3 of the LNA and mixer using an off-chip current setting resistor. The LNA IIP3 can be digitally controlled between two levels to reduce current draw in standby and other conditions where high IIP3 is not required. Noise Figure, IP3, and other specs are designed to be compatible with the CDMA, TDMA and GSM PCS communications. The IC is manufactured on an advanced Silicon Bipolar process and packaged in an SSOP-16 with an exposed die flag.



Optimum Technology Matching® Applied

- | | | |
|--|-----------------------------------|--------------------------------------|
| ☐ Si BJT | ☐ GaAs HBT | ☐ GaAs MESFET |
| ☒ Si Bi-CMOS | ☐ SiGe HBT | ☐ Si CMOS |



Functional Block Diagram

Package Style: SSOP-16EDF

Features

- Complete Receiver Front-End
- Adjustable LNA/Mixer Bias Current
- Adjustable LNA/Mixer IIP3

Ordering Information

- | | |
|-------------|---|
| RF2448 | PCS CDMA Low Noise Amplifier/Mixer 1500MHz to 2200MHz Downconverter |
| RF2448 PCBA | Fully Assembled Evaluation Board |

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Absolute Maximum Ratings

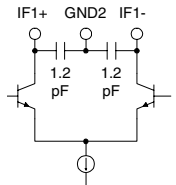
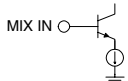
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V _{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



Caution! ESD sensitive device.

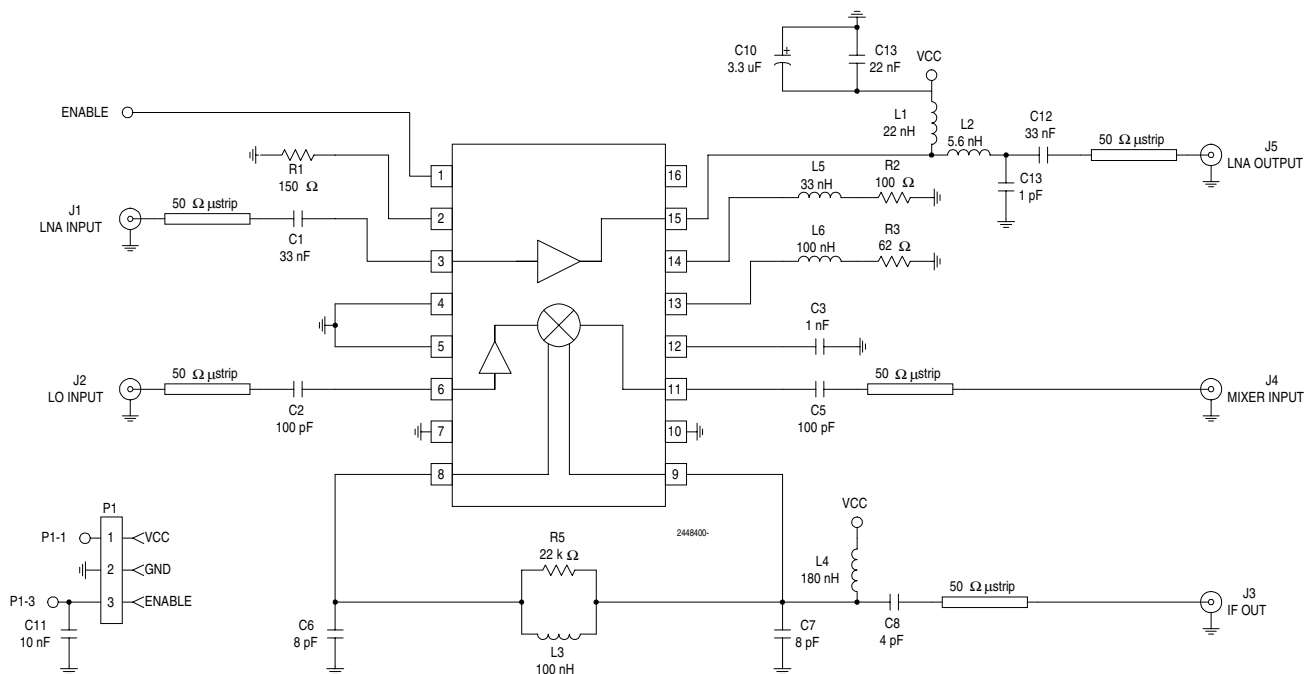
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T = 25°C, V _{CC} = 2.75V, RF = 1959MHz, LO = 1749MHz @ -2dBm
RF Frequency Range		1500 to 2200		MHz	
LO Frequency Range		1200 to 2200		MHz	
IF Frequency Range		0.1 to 250		MHz	
LNA					
Gain	13	14	15	dB	
Noise Figure		2.3		dB	
IIP3		+5.0		dBm	
Current at Max IIP3		5.0		mA	
Mixer					1 kΩ balanced load.
Gain		7.8		dB	
Noise Figure		11.5		dB	
IIP3		7.0		dBm	
RF to IF Isolation	40			dB	
Current		8.0		mA	
Local Oscillator Input					
Input Level	-10	-6	-4	dBm	
LO to IF Isolation	36			dB	
LO to LNA Isolation	35			dB	Any gain state.
Power Supply					
Voltage	2.65	2.75	3.9	V	

Pin	Function	Description	Interface Schematic
1	ENABLE	Power down control. This is a CMOS input. When this pin is CMOS "high" the device is enabled. When the level is CMOS "low" the device is shut off and a controlled attenuator is turned on.	
2	LNA ISET	This pin sets the current for the device. A resistor to ground of 1 k Ω provides a current of 17.5mA. The condition for optimal IP3 is to use the internal current setting option and leave this pin open (no connect).	
3	LNA IN	RF input pin. This pin is not internally DC blocked and requires an external blocking capacitor.	
4	LNA GND1	Ground connection for the LNA. Keep traces physically short and connect immediately to ground plane for best performance.	
5	LNA GND2	Ground connection for the bias circuits.	
6	LO IN	Mixer LO Balanced Input Pin. For single-ended input operation, this pin is used as an input and pin 18 is bypassed to ground.	
7	GND	Ground connection.	
8	IF1 OUT	CDMA IF Output pin. This is a balanced output. The internal circuitry, in conjunction with an external matching/bias inductor to V _{CC} , sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, at 210MHz is higher than 1 k Ω , even though the part is designed to drive a 1 k Ω load. Because this pin is biased to V _{CC} , a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
9	IF2 OUT	Same as pin 8, except complementary output.	See pin 8.
10	GND	Ground connection.	
11	MIX IN	Mixer RF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. External matching network sets RF and IF impedance for optimum performance.	
12	MIX CAP	Bypass capacitor for mixer.	
13	MIX ISET	This pin is used to set the bias current and IIP3 of the mixer buffer amplifier using a resistor to ground.	
14	LO ISET	This pin is used to set the bias current for the LO buffer amplifier using a resistor to ground.	
15	LNA OUT	LNA Output pin. This pin is internally DC blocked and externally matched to 50 Ω in order to facilitate an easy interface to a 50 Ω Image Filter.	See pin 2.
16	VCC	Power supply for the bias circuits.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

Evaluation Board Schematic

(Download [Bill of Materials](http://www.rfmd.com) from www.rfmd.com.)



Evaluation Board Layout Board Size 1.5" x 1.5"

Board Thickness 0.056", Board Material FR-4, Multi-Layer

