RF MICRO·DEVICES

Preliminary

RF2906

433MHZ PSK/FSK/ASK DATA TRANSCEIVER

Typical Applications

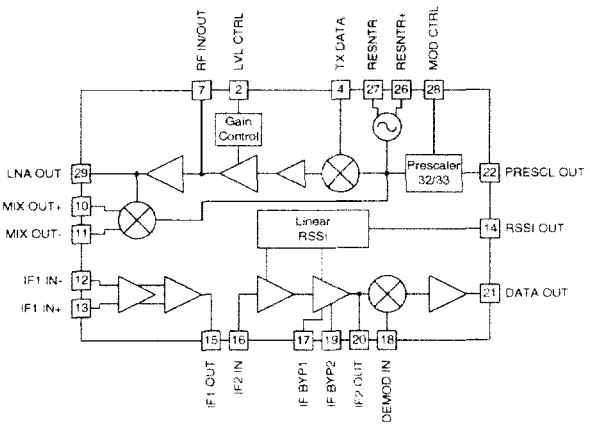
- Wireless Meter Reading
- Keyless Entry Systems
- Remote Controls
- Wireless Data Transceiver
- 433MHz European ISM Band Equipment
- Battery Powered Portable Devices

Product Description

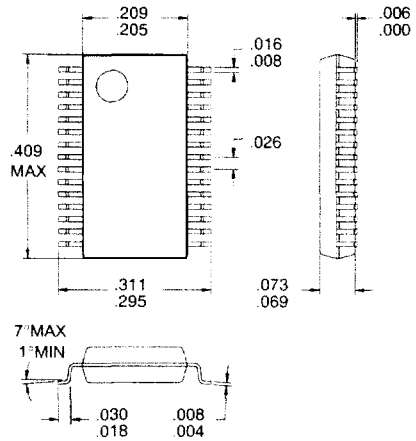
The RF2906 is intended for use in low power wireless applications operating in the radio frequency range of 100MHz to 600MHz. As a primary application, the RF2906 has been designed to operate as a FSK transceiver. A highly integrated device, it contains both transmit and receive radio functions, and by design no RX/TX switch is needed. The RF2906 features Phase Shift Keying (PSK), FSK, ASK,OOK,FM and AM modulation and demodulation capability. The part also includes a dual modulus (32/33) prescaler and VCO that can be used in conjunction with an external PLL IC to provide a synthesized LO. The transmitter features analog variable output power up to +10dBm from a 3.6V supply, and +8.5dBm from 3.0V. The chip includes provisions for full sleep mode.

Optimum Technology Matching® Applied

☑ Si BJT ☐ GaAs HBT ☐ GaAs MESFET
☐ Si Bi-CMOS



Functional Block Diagram



Package Style: SSOP-30

Features

- Fully Integrated UHF Transceiver
- 2.7V to 5.5V Supply Voltage
- PSK, FSK, ASK, OOK, FM, AM Capable
- Very Low Receive Current of 4.6mA
- Up to -97dBm Receive Sensitivity
- 10mW Output Power With Power Control

Ordering Information

RF2906	433MHz PSK/FSK/ASK Data Transceiver
RF2906 PCBA	Fully Assembled Evaluation Board

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11 TRANSCEIVERS

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+15	dBm
Output Load VSWR	20:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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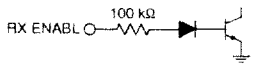
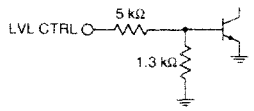
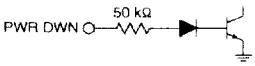
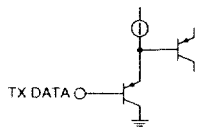
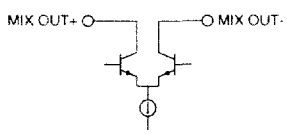
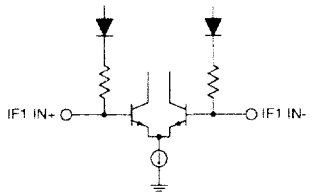
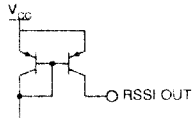
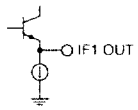
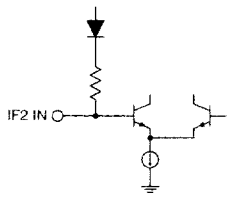
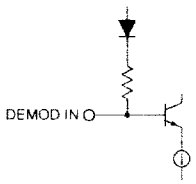
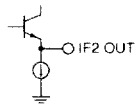
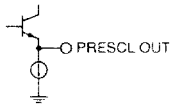
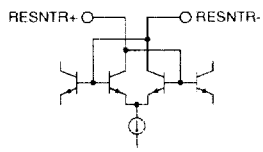
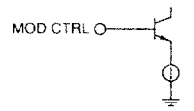
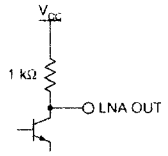
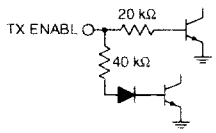
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=3.0V, Freq=433MHz
RF Frequency Range	30	433	600	MHz	
VCO and Prescaler					
VCO Frequency Range	30	433	600	MHz	
Prescaler Divide Ratio		32/33			
Prescaler Output Impedance	270	330	390	Ω	
Transmit Section					
TX Data Frequency	0.1	10	2000	kHz	
Modulator Input Impedance	1.6k	2k	2.4	Ω	
Maximum Power Level	+6	+8.5	+11	dBm	
	+7.5	+10	+12.5	dBm	V_{CC}=3.6V
Power Control Range	16	19		dB	
Power Control Sensitivity		6		dB/V	
Antenna Port Impedance		50		Ω	
Antenna Port VSWR		1.5:1	2.0:1		TX Mode f=433MHz
Carrier Suppression	15	22		dB	100kHz square wave data input, LVL CTRL="open"
Spurious Emissions	Compliant with the 433.05 to 434.79MHz European ISM band.				See Application Schematics.
Second Harmonic		-37	-34	dBm	With external filter, Pout=+8.5dBm
Third Harmonic		-38	-35	dBm	With external filter, Pout=+8.5dBm
Fourth Harmonic		-60	-63	dBm	With external filter, Pout=+8.5dBm
Fifth Harmonic		-65	-62	dBm	With external filter, Pout=+8.5dBm
Overall Receive Section					
Frequency Range	30	433	600	MHz	
LO Leakage at RF IN/OUT		-65	-62	dBm	
Cascaded Noise Figure		10		dB	
RX Sensitivity	-90	-97		dBm	IF BW=150kHz, Freq=433MHz, FM Deviation=50kHz, Data Rate=3kHz, DATA OUT S/N=6dB; DATA OUT_{High}>0.8*V_{CC} DATA OUT_{Low}>0.2*V_{CC}

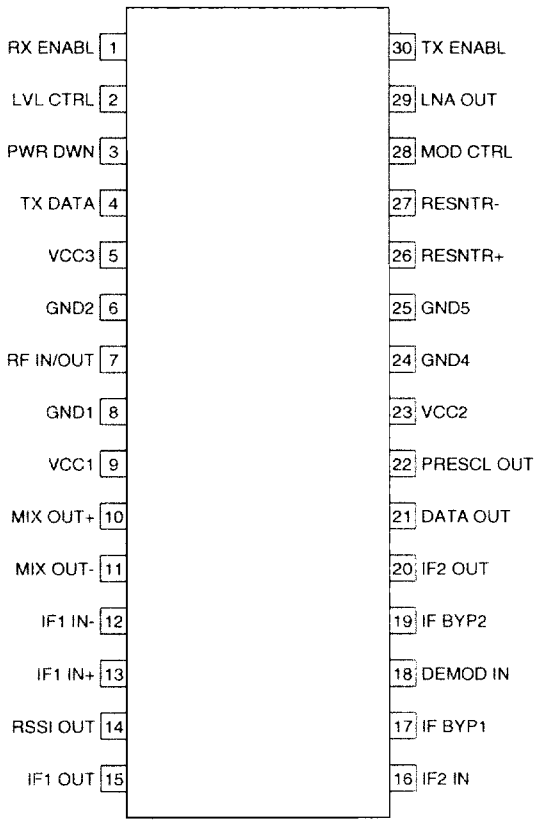
Receive Input Section					
Conversion Voltage Gain	15	18	21	dB	Differential mixer output
Noise Figure		10		dB	
Input IP_3		-27		dBm	
Antenna Port Impedance		50		Ω	
Antenna Port VSWR		1.5:1	2.0:1		RX Mode
Mixer Output Impedance		Open Collector		Ω	Actual impedance is set by the external components
First IF Section					
IF Frequency Range	0.4		11	MHz	
Voltage Gain	24	27	30	dB	IF=10.7MHz
IF1 Input Impedance	20k	25k	30k	Ω	
IF1 Output Impedance	280	350	420	Ω	
Second IF Section					
Voltage Gain	27	30	33	dB	IF=10.7MHz
RSSI DC Output Range		0.6 to 1.9		V	Pin=-110dBm to -55dBm
RSSI Sensitivity		37		mV/dB	Pin=-100dBm to -65dBm
RSSI Linear Range	30	35		dB	
IF2 Input Impedance	20k	25k	30k	Ω	
IF2 Output Impedance	120	150	180	Ω	
Demod Input Impedance	12k	15k	18	Ω	
Output Level	0.5		2.8	V	V_{CC}=3.0V, R_{LOAD}=1MΩ
Power Down Control					
Controls "ON"			2.0	V	Threshold voltage
Controls "OFF"	1.0			V	Threshold voltage
Control Input Impedance	25k	100k		Ω	
Turn On Time			1	ms	Dependent on the PLL loop bandwidth
Turn Off Time			1	ms	Dependent on the PLL loop bandwidth
RX to TX and TX to RX Time			100	µs	Dependent on the PLL loop bandwidth
Power Supply					
Voltage		3.0		V	Specifications
	2.7		5.0	V	Operating limits
Current Consumption	20	27	35.5	mA*	TX Mode, P_{OUT}=+8.5dBm
	11	14	17	mA	TX Mode, P_{OUT}=0dBm
	3	4.6	6	mA*	RX Mode
			1	µA*	Power Down Mode
	1.5	3	4	mA*	Locked Mode
					*100% Tested Parameter.Guaranteed Limits.

Pin	Function	Description	Interface Schematic
1	RX ENABL	Enable pin for the receiver circuitry. This is a digitally controlled input. A logic "high" turns the receiver on. A logic "low" disables the receiver.	
2	LVL CTRL	Analog gain control pin for the PA. Maximum gain occurs when the voltage at this pin is 0V. Minimum gain occurs when the voltage at this pin is V_{CC}.	
3	PWR DWN	Power down control for the entire chip. A logic "high" enables the circuits and a logic "low" disables all functions.	
4	TX DATA	Input to the transmitter digital modulator (High Impedance). This input is used for PSK applications. For FSK applications the TX data is applied to an external varactor diode in the VCO tank circuit (see Application schematic) and the TX DATA pin should be tied to ground.The DC voltage supplied to this pin should be $V_{CC}/2$. The input to this pin should be a standard TTL/CMOS Logic level.	
5	VCC3	Supply voltage for the PA. External bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect directly to the ground plane.	
6	GND2	Ground connection for the IF, RSSI, baseband and PA circuitry. Connect directly to the ground plane.	
7	RF IN/OUT	RF input/output pin. Provides RF input to the LNA when the receiver is enabled and the transmitter is disabled. Provides RF output from the PA when the receiver is disabled and the transmitter is enabled. This pin requires an external DC blocking capacitor.	
8	GND1	Ground connection for the LNA. Connect directly to the ground plane.	
9	VCC1	Main supply voltage for the chip including voltage reference #1. External bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect directly to the ground plane.	
10	MIX OUT+	RF mixer output. Pins 10 and 11 are open collector, complementary outputs. These pins must be connected to V_{CC} through an inductor to provide DC bias for the mixer. The inductance at these pins should be parallel resonated with a resistor and a capacitor to form a bandwidth limiting tank circuit (see application circuit). The tank resistance will set the Q of the filter and the gain of the mixer.	
11	MIX OUT -	Complementary output of MIX OUT+.	See pin 10.
12	IF1 IN-	First balanced input to IF amplifier 1 (High Impedance). This pin requires an external DC blocking capacitor.	
13	IF1 IN+	Complementary input of IF IN-	See pin 12.
14	RSSI OUT	Received signal strength indicator. High impedance, current source output. The DC current supplied by this pin is proportional to the signal level (in dB) present in all three IF amplifiers.	

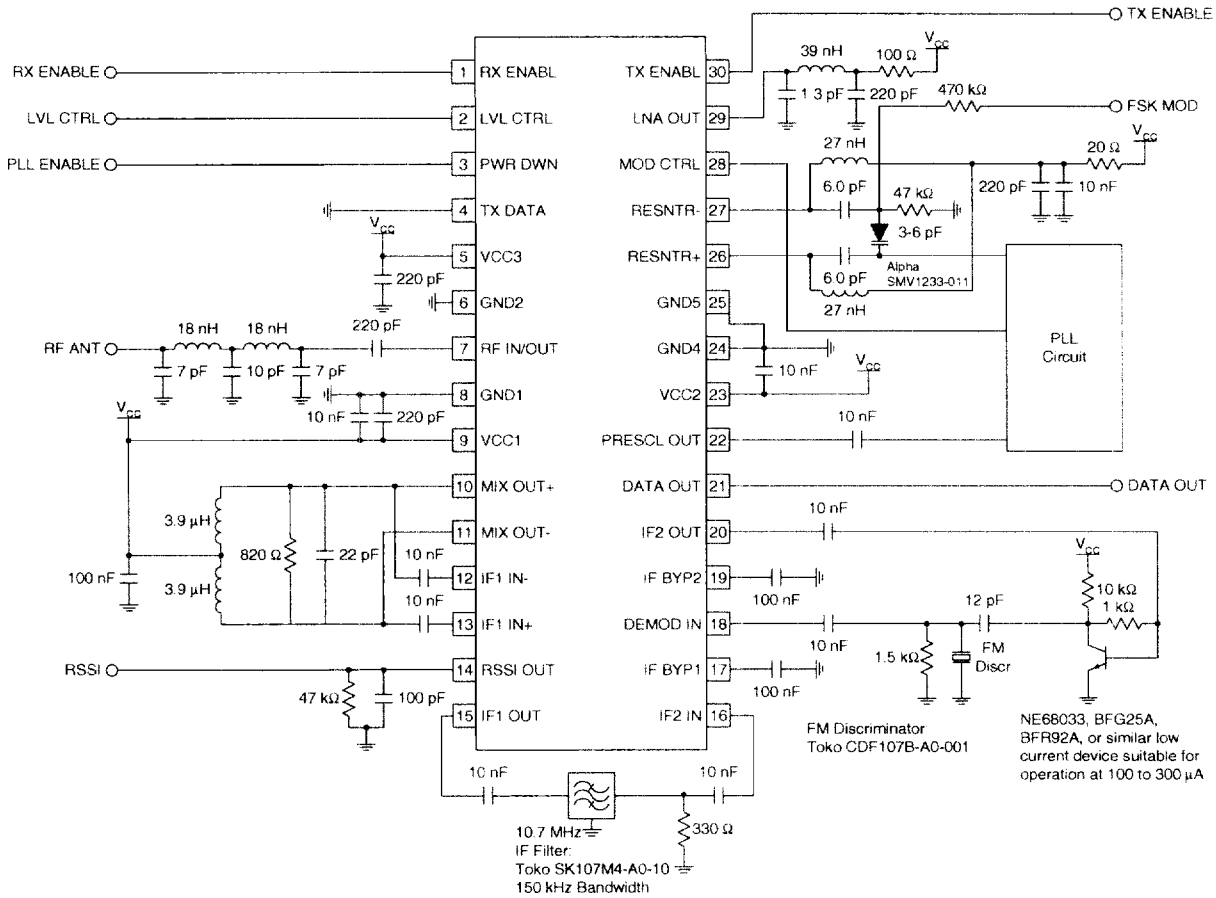
15	IF1 OUT	Single ended output of IF amplifier 1. The output impedance at this pin is approximately 500Ω. This pin requires an external DC blocking capacitor.	
16	IF2 IN	Single ended input to the second IF amplifier. This pin requires an external DC blocking capacitor.	
17	IF BYP1	Bypass connection for the DC feedback of the high gain limiter stage. A large decoupling capacitor is required at this node.	
18	DEMOD IN	Demodulator input. This pin requires an external DC blocking capacitor.For FSK/FM applications a quadrature tank/discriminator is connected to this pin.For BPSK applications the recovered carrier input level in coherent applications should be in the range of -27dBm to -33dBm (referenced to a 50Ω source) for optimum performance.	
19	IF BYP2	Bypass connection for the DC feedback of the high gain limiter stage. A large decoupling capacitor is required at this node.	
20	IF2 OUT	Single ended output of the second IF amplifier. The output impedance at this pin is approximately 150Ω. This pin requires an external DC blocking capacitor. This signal can be used to generate the quadrature signal component for FSK/FM detection by feeding it to a quadrature tank/discriminator and then to the DEMOD IN.	
21	DATA OUT	Demodulated data output pin. This is a current mode output that can sink or source approximately 20μA.	
22	PRESCL OUT	Prescaler output pin. Output level is 900mV$_{PP}$ into a 5pF capacitive load at F_{MAX}. The output impedance of this pin is approximately 330Ω.	
23	VCC2	Supply voltage for the prescaler and voltage reference #2. External bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect directly to the ground plane.	
24	GND4	Ground connection for the prescaler, VCO and power control circuitry. Connect directly to the ground plane.	
25	GND5	Ground connection for the mixer, modulator and PA buffer. Connect directly to the ground plane.	
26	RESNTR+	VCO tank connection. Pins 24 and 25 are open collector, complementary outputs. These pins must be connected to V_{CC} through an inductor to provide DC bias for the VCO. The inductance at these pins should be connected in parallel with a varactor to form a voltage controlled resonant tank circuit (see application circuit).	
27	RESNTR-	See RESNTR+ description.	

28	MOD CTRL	Control pin for the modulus of the prescaler. This is a digital control pin. A logic "low" at this pin forces the prescaler to divide by 33. A logic "high" at this pin forces the prescaler to divide by 32.	
29	LNA OUT	LNA output/RF Mixer Input pin. A parallel resonator tuned at the RF input frequency should be connected to V_{CC} as shown in the application circuit.	
30	TX ENABL	Enable pin for the transmitter circuitry. This is a digitally controlled input. A logic "high" turns the transmitter on. A logic "low" disables the transmitter.	

Pin Out

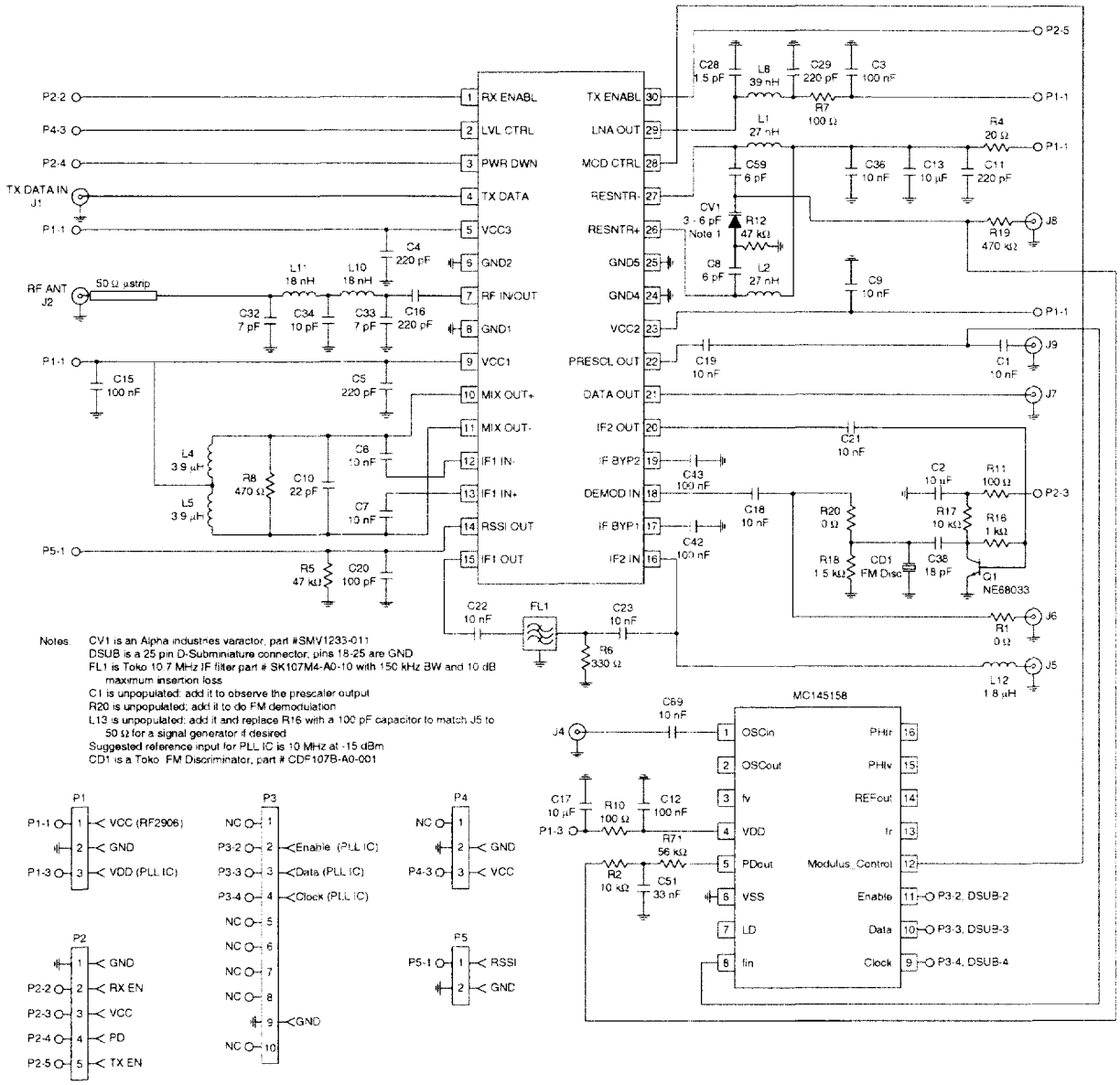


Application Schematic
FSK Modulation

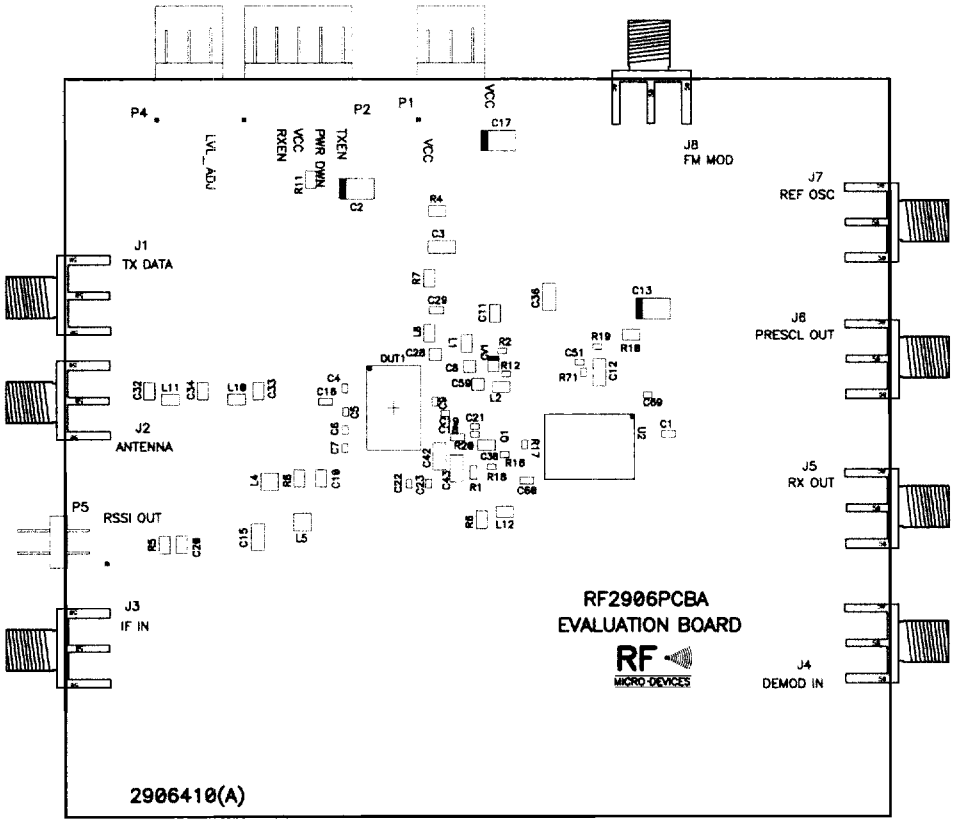


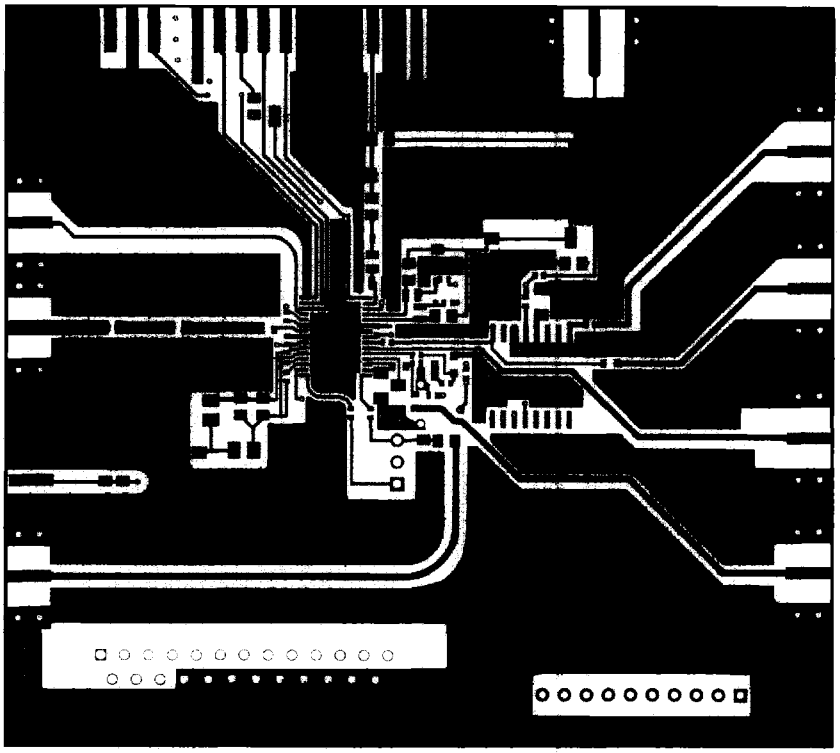
Evaluation Board Schematic

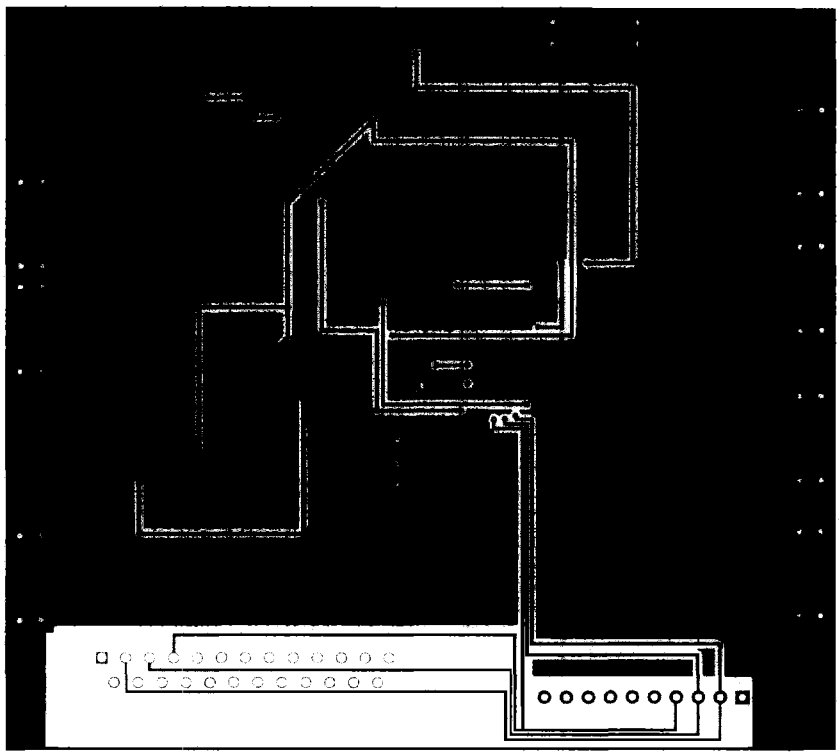
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
3.768 x 3.393"
(Assembly, Top Layer, Bottom Layer)







RSSI Output vs. Input Power