RF2909

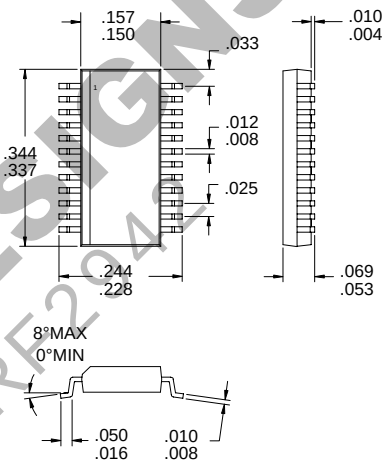
3V 915MHZ SPREAD-SPECTRUM TRANSMITTER IC

Typical Applications

- Direct Sequence Spread Spectrum
- Spread Spectrum Cordless Phones
- Portable Battery Powered Equipment
- GMSK, QPSK, DQPSK, QAM Modulation
- 915MHz ISM Applications

Product Description

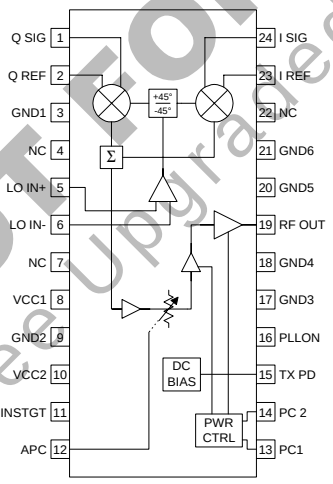
The RF2909 is a monolithic integrated transmitter IC capable of universal direct modulation. The quadrature modulator allows for a variety of modulation formats and compound carriers. The transmitter has two power control modes. Two inputs can be controlled digitally for stepping output power 1mW, 10mW, or 70mW output power. Or, the output level can be adjusted by an analog input from 1mW to 80mW. The quadrature mixers have differential inputs, and are internally biased; a DC blocking capacitor is required if external DC levels are present. The LO is split with a passive network tuned for 915MHz.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- 2.7V to 5V Power Supply
- 1mW, 10mW, 70mW Digital Output Power
- 20dB Analog Power Control Range
- Excellent Phase & Amplitude Balance
- Compatible with the RF2908

Ordering Information

RF2909	3V 915MHz Spread-Spectrum Transmitter IC
RF2909 PCBA	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Power Down Voltage (V_{PD})	V_{DD}+0.4	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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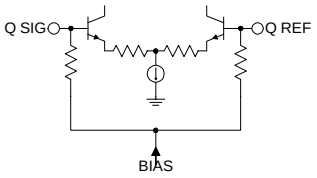
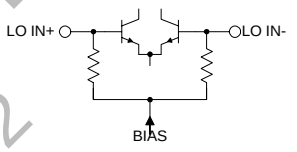
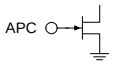
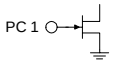
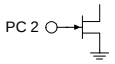
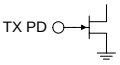
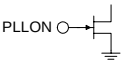
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Carrier Input (LO IN)					T=25°C, V_{DD}=3.3V
Frequency Range	100	902-928	1100	MHz	Phase shift optimized for 915MHz
Power Level		-10		dBm	Differential
Input Impedance		50		Ω	915MHz
Modulation Input					
Frequency Range	DC	10	500	MHz	50Ω source, I,Q=500mV_{p-p}
Reference Voltage (V_{REF})		1.7		V	
Modulation for P_{OUT} Power (I & Q)		500		mV_p	Differential, 1V_p single ended
Maximum Modulation (I & Q)		1		V_p	Differential, 1.5Vp single ended
Quadrature Phase Error		3	5	°	
I/Q Amplitude Imbalance		.35		db	
Input Impedance		3		kΩ	Differential
RF Output					V_{DD}=3.3V, LO power=-10dBm, LO frequency=915MHz, SSB, I/Q=1V_{PP} sine wave, 100KHz
Digital Output Power		1, 10, 70		mW	See Table I for control logic
Output Impedance		50		Ω	
Output VSWR			1.5:1		With external matching (see app. schematic)
Second Harmonic Output		-25		dBc	
Other Harmonics Output		-30		dBc	
Sideband Suppression		30		dB	P_{OUT}=10mW
Carrier Suppression		27		dB	Modulation DC offset can be externally adjusted for optimum suppression. Carrier suppression is then typically better than 40dB.
Output Level Control					
Analog Power Control Range	20			dB	
Analog Power Control Voltage (APC)	0		3.6	V	Input voltage to pin 12 must be less than 3.6V or V_{CC} (whichever is less).
Analog Power Control Input Current			1	µA	
Analog Power Output		80		mW	V_{APC}=2.8V, PC1="0", PC2="0"
Digital Power Output, High		70		mW	APC=0V, PC 1="0", PC 2="1"
Digital Power Output, Med		10		mW	APC=0V, PC 1="1", PC 2="0"
Digital Power Output, Low		1		mW	APC=0V, PC 1="0", PC 2="0"
PC 1/PC 2 "ON"			1		Threshold Voltage
PC 1/PC 2 "OFF"	2				Threshold Voltage
Standby Mode					
Turn On/Off Time		0.15	1	µS	
Power Down "ON"	2			V	Threshold voltage; Part is turned "ON"
Power Down "OFF"			1	V	Threshold voltage; Part is turned "OFF"

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Supply					
Voltage		3.3		V	Specifications
	2.7		5.0	V	Operating limits
Current		175	200	mA	Total, Digital High Power, V_{APC}, V_{PC1}=0V, V_{PC2}=V_{CC}
		45	60		Total, Digital Medium Power, V_{APC}, V_{PC2}=0V, V_{PC1}=V_{CC}
		30	40	mA	Total, Digital Low Power, V_{APC}, V_{PC1}, V_{PC2}=0V
		130	180	mA	Total, Linear Power, V_{APC}=2.8V, V_{PC1}, V_{PC2}=0V
		1.5	5	mA	PLL Buffer amp on.
			1	µA	Standby mode

Pin	Function	Description	Interface Schematic
1	Q SIG	Baseband input to the Q mixer. A DC bias of approximately 1.7V is present at this pin.A DC blocking capacitor is needed if the signal has a different DC level. Maximum output power is obtained when the input signal has a peak-to-peak amplitude of 1V. The input impedance of this pin is 3kΩ. The REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. The SIG and REF pins may be driven deferentially to increase conversion gain.	
2	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ±0.15V (relative to the Q SIG DC voltage). Without tuning, the carrier suppression will typically be better than 25dB. The input impedance of this pin is about 3 kΩ.	See pin 1.
3	GND 1	Ground connection for the modulator circuits. Keep traces physically short and connect immediately to ground plane for best performance.	
4	NC		
5	LO IN+	Balanced LO Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The balanced input impedance is 100Ω. The single-ended input impedance is 50Ω.	
6	LO IN-	Same as pin 4, except complementary input.	See pin 5.
7	NC		
8	VCC1	This pin is used to supply V_{CC} to the modulator circuits. A RF bypass capacitor should be connected directly to this and ground.	
9	GND2	Ground connection. This pin is used for RF ground of the power control circuitry and the PA driver amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
10	VCC2	This pin is used to supply V_{CC} to the power control and pre amp circuitry. A RF bypass capacitor should be connected directly to this and ground.	
11	INSTGT	Interstage bias point between pre amp and power amp. This pin should be pulled up to V_{CC} with an 8.2nH inductor for 915MHz.	See pin 18.
12	APC	Analog power control input. This pin can be used as a linear power output control with a range of 20 dB. Maximum output power is achieved when APC is high. APC is"wire-or'd" with the digital controls, therefore should be low when using the digital control. The DC input voltage to the pin should always be less than 3.6V.	
13	PC 1	This digital power control input sets the medium current and power output, 10mW. It is "wire-or'd" with APC and PC 2 and can be overcome by either. Therefore, APC and PC 2 must be low to use this setting.	
14	PC 2	This digital power control input set the high current and power output, 100mW. It is "wire-or'd" with APC and PC 1 and can override both of those controls. Therefore, PC 2 must be low to use other settings.	
15	TX PD	Enables all of the IC except for the LO buffer when > 2V.	
16	PLLON	Enables the LO buffer amp when > 2V.This can be switched on and off independently of the rest of the IC. This amp draws 1.5mA typically.This can be used to minimize load pulling of the VCO when the transmitter is turned on. Buffer amp is off when < 1V.	
17	GND3	Ground connection for RF Power Amp. Keep traces physically short and connect immediately to ground plane for best performance.	
18	GND4	Same as pin16.	

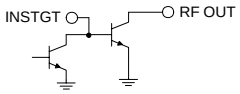
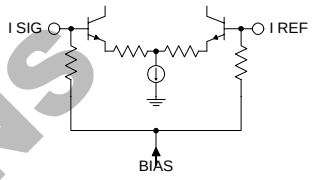
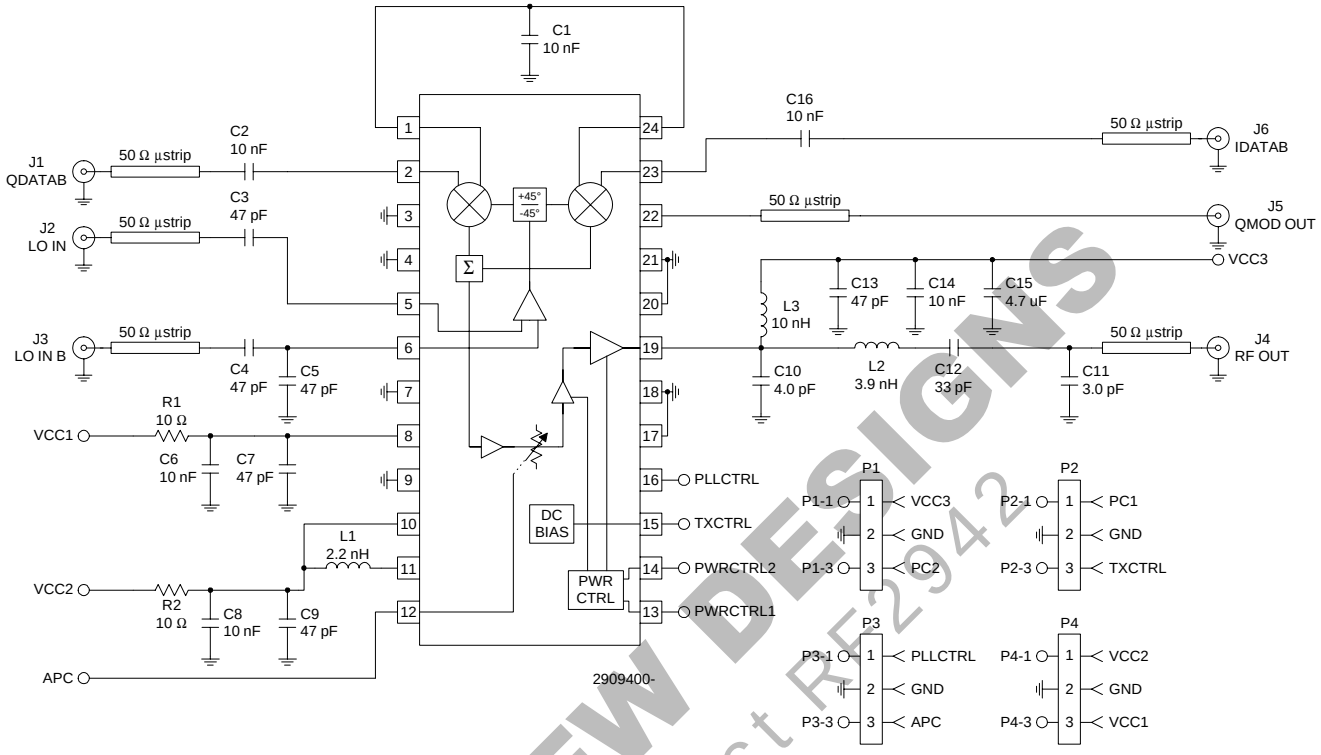
Pin	Function	Description	Interface Schematic
19	RF OUT	Power Amp output, open collector output.	
20	GND5	Same as pin 17.	
21	GND6	Same as pin 17.	
22	NC		
23	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ±0.15V (relative to the I SIG DC voltage). Without tuning, the carrier suppression will typically be better than 25dB. The input impedance of this pin is 3kΩ.	
24	I SIG	Baseband input to the I mixer. A DC bias of approximately 1.7V is present at this pin.A DC blocking capacitor is needed if the signal has a different DC level. Maximum output power is obtained when the input signal has a peak to peak amplitude of 1V. The input impedance of this pin is about 3 kΩ. The REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. The SIG and REF pins may be driven differentially to increase conversion gain.	See pin 23.

Table I

Operation Mode	TX PD	PLL ON	PC 1	PC 2	APC	Function
Sleep Mode	Low	Low	Low	Low	0V	Entire chip is powered down. Total I_{cc}<1μA.
PLL Buffer	Low	High	Low	Low	0V	LO Buffer is on. I_{cc}=1.5mA
Linear Po Mode	High	High	Low	Low	0-V_{cc}V	Transmitter in on. Power output is proportional to APC.
Digital Po Mode	High	High	Low	Low	0V	Transmitter is on. Power out is 1mW.
Medium Power	High	High	High	Low	0V	Transmitter is on. Power out is 10mW.
High Power	High	High	Low	High	0V	Transmitter is on. Power out is 70mW.

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1.7440" x 1.7480"