RF9906

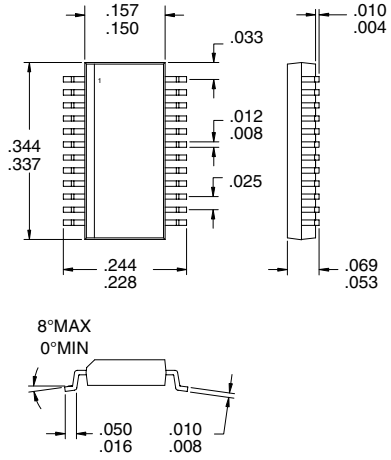
CDMA/FM LOW NOISE AMPLIFIER/MIXER

Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Down Converter
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

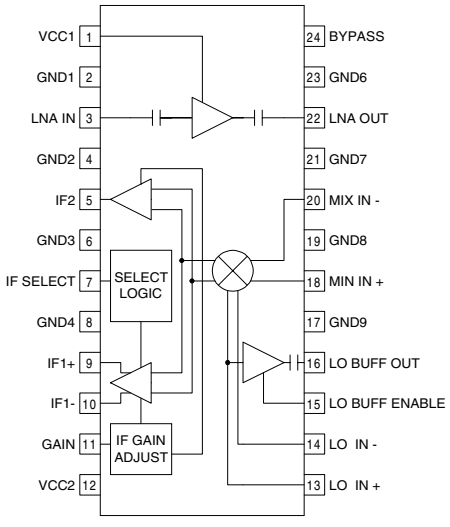
The RF9906 is a receiver front-end designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to amplify and down-convert RF signals while providing 9dB of gain control range. Noise Figure, IP3, and other specs are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of this Receive LNA/Mixer, a Receive IF AGC Amp, a Transmit IF AGC Amp, and a Transmit Upconverter. The IC is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and is packaged in a standard miniature 24-lead plastic SSOP package.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Complete Receiver Front-End
- Analog Gain Control
- Single 3.6V Power Supply
- Buffered LO Output
- Digitally Selectable IF Outputs
- 500MHz to 1500MHz Operation

Ordering Information

RF9906	CDMA/FM Low Noise Amplifier/Mixer
RF9906 PCBA	Fully Assembled Evaluation Board

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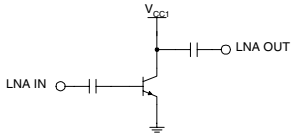
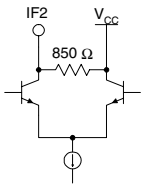
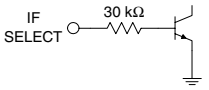
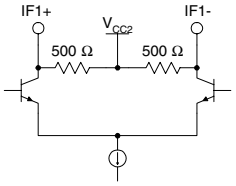
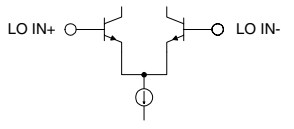
Absolute Maximum Ratings

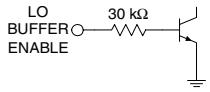
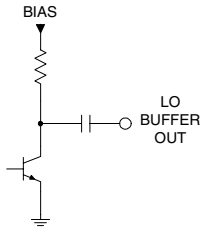
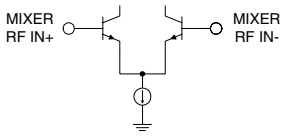
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input LO and RF Levels	+3	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

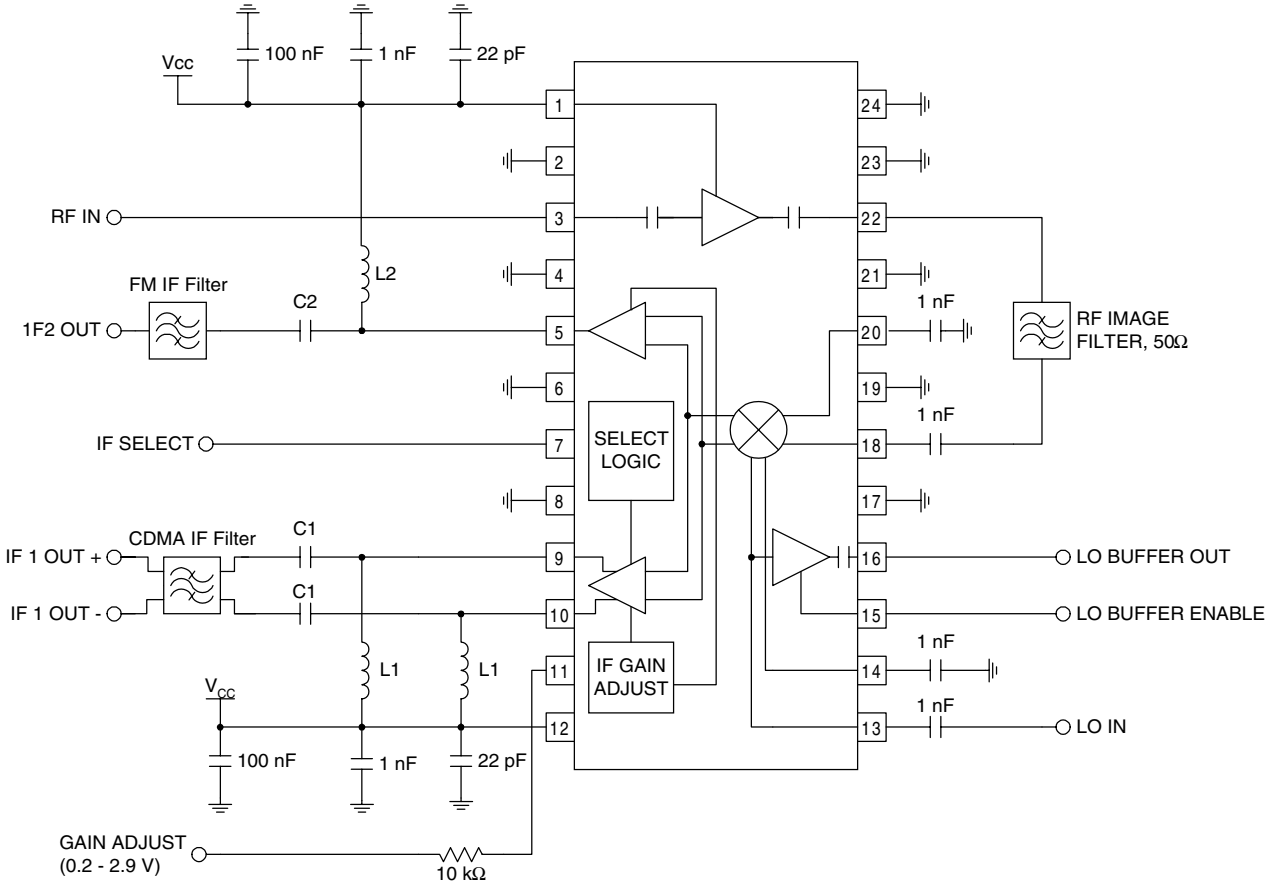
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, RF=881MHz, LO=966MHz @ -5dBm
RF Frequency Range		500 to 1500		MHz	
LO Frequency Range		500 to 1500		MHz	
IF Frequency Range		0.1 to 250		MHz	
Cascaded Performance to IF1					CDMA Mode, IF SEL.=2.9V, 1kΩ balanced load, 2.5dB Image Filter Loss. By varying the gain of the second stage, a trade-off of gain and noise figure against IP3 can be made.
Cascade Conversion Gain, Maximum	27.5	30	33	dB	$V_G \leq 0.2V$
Cascade Conversion Gain, Minimum		21		dB	$V_G \geq 2.5V$
Cascade IP3	-15	-13		dBm	Referenced to input at Maximum Gain
Cascade Noise Figure		2.6	3.4	dB	Single sideband, at Maximum Gain Setting
Cascaded Performance to IF2					FM Mode, IF SEL.=0V, 850Ω load, 2.5dB Image Filter Loss. By varying the gain of the second stage, a trade-off of gain and noise figure against IP3 can be made.
Cascade Conversion Gain, Maximum	18.5	21	24	dB	$V_G \leq 0.2V$
Cascade Conversion Gain, Minimum		12		dB	$V_G \geq 2.5V$
Cascade IP3	-15	-12.5		dBm	Referenced to input at Maximum Gain
Cascade Noise Figure		3.0	4.0	dB	Single sideband, at Maximum Gain Setting
First Section (LNA)					The LNA section may be left unused. Power is not connected to pin 1. The performance is then as specified for the Second Section (Mixer).
Noise Figure		1.5		dB	
Input VSWR		<1.5:1			
Input IP3		-8		dBm	
Gain		16		dB	
Reverse Isolation		23		dB	
Output VSWR		<1.5:1			

Second Section (Mixer, IF1 Output)					With 1kΩ balanced load. By varying the gain of the second stage, a trade-off of gain and noise figure against IP3 can be made. Please see data plots.
Noise Figure		9.5		dB	Single Sideband
Input VSWR		1.5:1			Single-ended
Input IP3		+2		dBm	At maximum gain
Conversion Gain, Maximum		16.5		dB	$V_G \leq 0.2V$
Conversion Gain, Minimum		5.5		dB	$V_G \geq 2.5V$
Output Impedance		1		kΩ	Balanced
Second Section (Mixer, IF2 Output)					With 850Ω load. By varying the gain of the second stage, a trade-off of gain and noise figure against IP3 can be made. Please see data plots.
Noise Figure		11		dB	Single Sideband
Input VSWR		1.5:1			Single ended
Input IP3		+2		dBm	At maximum gain
Conversion Gain, Maximum		7.5		dB	$V_G \leq 0.2V$
Conversion Gain, Minimum		-4.5		dB	$V_G \geq 2.5V$
Output Impedance		850		Ω	Single ended
LO Input					
LO Input Range		-6 to 0		dBm	
LO Output Level	-7.5	-5	-2.5	dBm	Buffer On, -5dBm input
LO Output Level		-35	-30	dBm	Buffer Off, -5dBm input
LO to RF (Mix In) Rejection		27		dB	
LO to IF1, IF2 Rejection		20		dB	
LO Input VSWR		<2:1			Single ended
Power Supply					
Voltage		3.6±5%		V	
Current Consumption		7		mA	LNA only
		41.5	58	mA	LNA + Mixer, IF1, LO Buffer On
		39	55	mA	LNA + Mixer, IF1, LO Buffer Off
		32.5	45	mA	LNA + Mixer, IF2, LO Buffer On
		30	42	mA	LNA + Mixer, IF2, LO Buffer Off

Pin	Function	Description	Interface Schematic
1	VCC1	Supply voltage for the LNA. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	LNA IN	RF input pin. This pin is internally DC blocked and matched to 50Ω.	
4	GND	Same as pin 2.	
5	IF2	FM IF output pin. This is a single-ended output with an output impedance set by an internal 850Ω resistor to V_{CC}. The resistor sets the operating impedance, but an external choke or matching inductor to V_{CC} must be supplied in order to correctly bias this output. This inductor is typically incorporated in the matching network between the output and IF filter. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground.	
6	GND	Same as pin 2.	
7	IF SELECT	Selects which IF output (IF1 or IF2) is used. This is a digitally controlled input. A logic "high" selects IF1. A logic "low" selects IF2. The threshold voltage is approximately 1.3V.	
8	GND	Same as pin 2.	
9	IF 1+	CDMA IF output pin. This is a balanced output. The output impedance is set by an internal 500Ω resistor to V_{CC}. Thus the output impedance of each pin is 500Ω, whereas the differential output impedance is 1000Ω. The resistor sets the operating impedance, but an external choke or matching inductor to V_{CC} must be supplied in order to correctly bias this output. This inductor is typically incorporated in the matching network between the output and IF filter. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground.	
10	IF 1-	Same as pin 9 except complementary input.	See pin 9.
11	GC	Analog gain adjustment for both IF output buffer amplifiers. A 10kΩ source impedance is required for proper operation of the gain control circuitry. Valid control voltages, on the source side of the 10kΩ resistor, are from 0V to 2.9V. Minimum gain is selected with 2.4V to 2.9V. Maximum gain is selected with 0V to 0.2V. When operating the RF9906 at fixed maximum gain, this pin should be grounded through a 10kΩ resistor. Do not connect this pin directly to ground (see Application Schematic for example).	
12	VCC2	Supply Voltage for the Mixer, LO Buffer Amplifier, and IF Buffer Amplifiers. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
13	LO IN+	Mixer LO Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other mixer LO input is AC coupled to ground. The single-ended input impedance is 50Ω.	
14	LO IN-	Same as pin 13, except complementary input.	See pin 13.

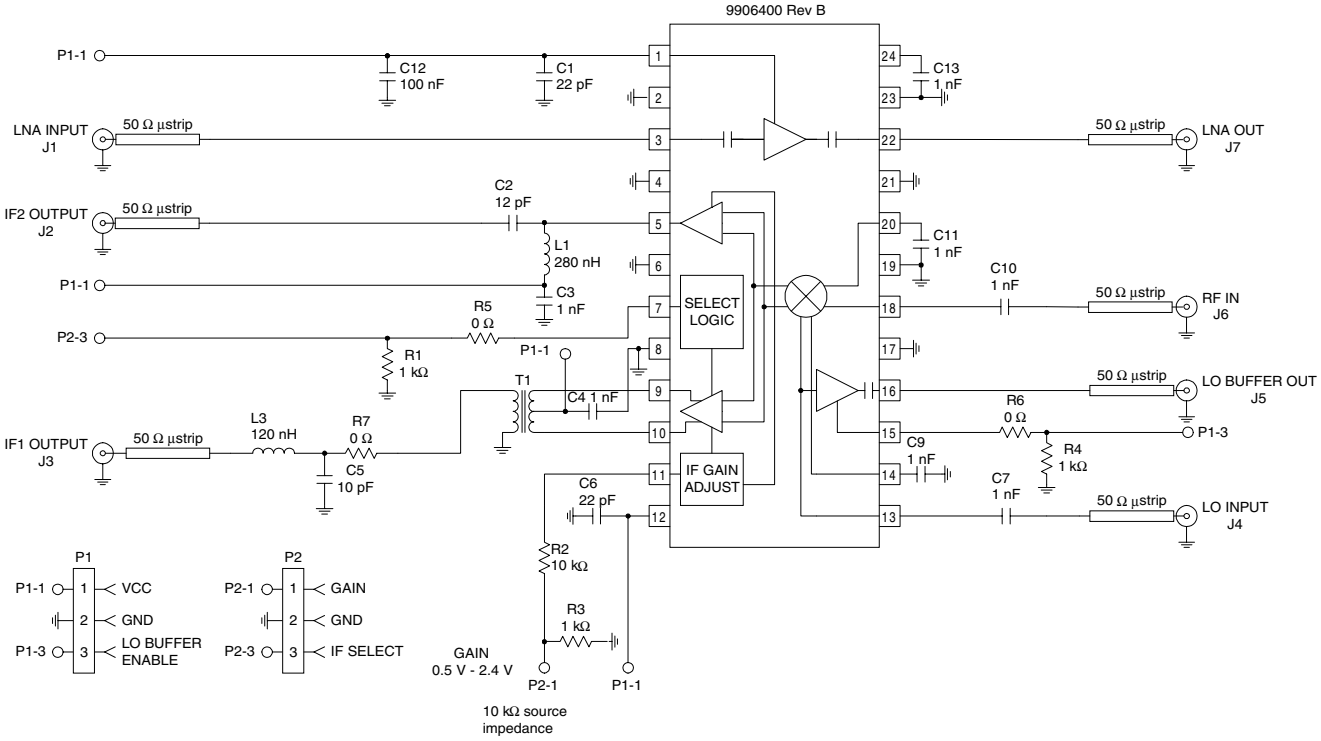
15	**LO BUFFER ENABLE**	Enable pin for the LO output buffer amplifier. This is a digitally controlled input. A logic "high" turns the buffer amplifier on, and the current consumption increases by 3mA (with -3dBm LO input). A logic "low" turns the buffer amplifier off. The threshold voltage is approximately 1.3V.	
16	**LO BUFFER OUT**	Optional Buffered LO Output. This pin is internally DC blocked and matched to 50Ω. The buffer amplifier is switched on or off by the voltage level at pin 15.	
17	**GND**	Same as pin 2.	
18	**MIXER RF IN+**	Mixer RF Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other mixer RF input is bypassed to ground. In order to minimize the mixer's noise figure, the bypass capacitor must be a low input impedance at the IF frequency. The single-ended input impedance is 50Ω.	
19	**GND**	Same as pin 2.	
20	**MIXER RF IN-**	Same as pin 18, except complementary input.	See pin 18.
21	**GND**	Same as pin 2.	
22	**LNA OUT**	LNA Output pin. This pin is internally DC blocked and matched to 50Ω in order to facilitate an easy interface to a 50Ω Image Filter.	See pin 3.
23	**GND**	Same as pin 2.	
24	**BYPASS**	IF circuitry bypass pin. This pin should be well bypassed at the IF frequency in order to achieve specified FM (IF2) noise figure. The ground side of the bypass capacitor should connect immediately to ground plane. 1000pF is the suggested value. Smaller values will begin to slightly degrade noise figure. Larger values will slow down the IF1 to IF2 switching times.	

Application Schematic



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout

Board Thickness 0.014”; Board Material FR-4 ????