

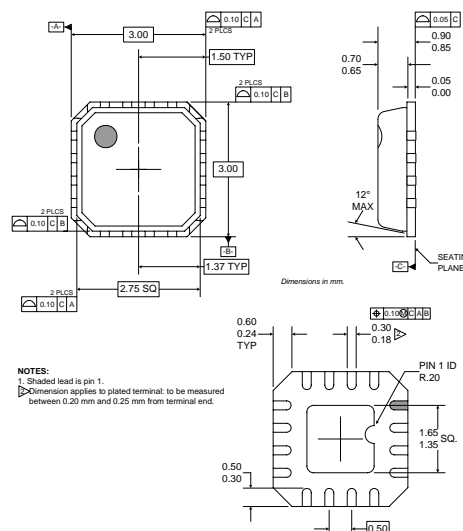
## RoHS Compliant & Pb-Free Product

### Typical Applications

- CDMA Korean PCS Systems
- CDMA US PCS Systems
- IMT-2000 and 2.4GHz Band Applications
- GPS Applications
- General Purpose Downconverter
- Commercial and Consumer Systems

### Product Description

The RF2860 is a broadband receiver front-end designed for CDMA PCS applications. The broadband design makes it a great solution as well for GPS, IMT-2000 and 2.4GHz applications. It is designed to amplify and down-convert RF signals, while providing 21.5dB of stepped gain control range. Features include digital control of LNA gain, TX buffer/enable, and power down mode. Another feature of the chip is the ability to set the bias point and RF performance of the LNA and mixer through the ISET1 and ISET2 resistors respectively. Noise figure, IIP3, and gain are designed to exceed the IS-98 interim standard requirement for CDMA PCS communications. The IC is manufactured on an advanced Silicon Germanium Bi-CMOS process and is in a 3mmx3mm, 16-pin, lead-less chip carrier.



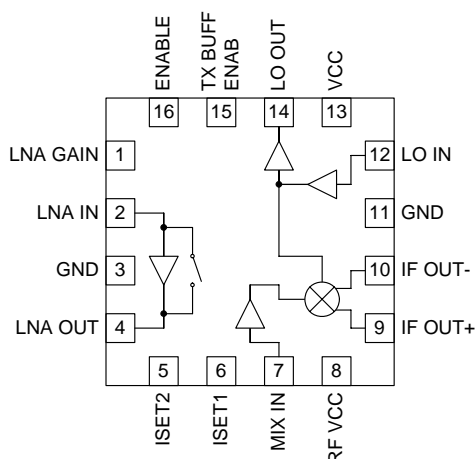
### Optimum Technology Matching® Applied

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|-------------------------------------|-----------------------------------|--|
| <input type="checkbox"/> Si BJT     | <input type="checkbox"/> GaAs HBT | <input type="checkbox"/> GaAs MESFET             |
| <input type="checkbox"/> Si Bi-CMOS | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si CMOS                 |
| <input type="checkbox"/> InGaP/HBT  | <input type="checkbox"/> GaN HEMT | <input checked="" type="checkbox"/> SiGe Bi-CMOS |

Package Style: QFN, 16-Pin, 3x3

### Features

- LNA Noise Figure=1.3dB (KPCS)
- Stepped LNA Gain Control
- Integrated TX LO Buffer Amplifier
- Adjustable IIP3 versus Current for both LNA and Mixer Blocks
- All Pins ESD Protected



Functional Block Diagram

### Ordering Information

RF2860      PCS CDMA Low Noise Amplifier/Mixer Broadband  
Downconverter  
RF2860PCBA-41X Fully Assembled Evaluation Board

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# RF2860

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V <sub>DC</sub>
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



**Caution!** ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall</b>					T = 25°C, V <sub>CC</sub> =2.75V
RF Frequency Range		1575 to 2170		MHz	
IF Frequency Range	0.1		400	MHz	
<b>Power Supply</b>					
Supply Voltage	2.65	2.75	3.15	V	
Logic High	1.8			V	
Logic Low			0.4	V	
Power Down Current			10	μA	ENABLE=0
<b>US PCS Band</b>					Freq=1930MHz to 1990MHz
<b>Korean PCS Band</b>					Freq=1840MHz to 1870MHz
<b>GPS Band</b>					Freq=1575.42MHz
<b>IMT-2000 Band</b>					Freq=2110MHz to 2170MHz
<b>LNA (On) - KPCS</b>					LNA 50Ω match
Gain	14.0	16.5	17.5	dB	
Noise Figure		1.3	1.5	dB	
Input IP3	+6.0	+8.0		dBm	
Current		6.5		mA	
Isolation		20		dB	
<b>LNA (On) - US PCS</b>					LNA 50Ω match
Gain	13.5	16.0	17.0	dB	
Noise Figure		1.4	1.6	dB	
Input IP3	+6.0	+8.0		dBm	
Current		6.5		mA	
Isolation		30		dB	
<b>LNA (On) - GPS Band</b>					LNA 50Ω match
Gain	14.75	17.25	18.25	dB	
Noise Figure		1.2		dB	
Input IP3		+5.0		dBm	
Current		6.0		mA	
Isolation		20		dB	
<b>LNA (On) - IMT-2000 Band</b>					LNA 50Ω match
Gain	12.0	14.5	15.5	dB	
Noise Figure		1.4		dB	
Input IP3		+8.0		dBm	
Current		6.0		mA	
Isolation		20		dB	
<b>LNA (Off) - US PCS, KPCS, GPS, IMT-2000</b>					
Gain	-6.5	-5.0	-3.5	dB	
Noise Figure		5.0	6.0	dB	
Input IP3	+20.0	+25.0		dBm	
Current		0		mA	
Isolation		4		dB	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
US PCS Band, Korean PCS Band, GPS Band, IMT-2000 Band, cont'd					
Mixer - KPCS/US PCS					See note.
Gain	12.0	14.0	15.5	dB	
Noise Figure		7.0	8.0	dB	
Input IP3	+1.0	+3.0		dBm	
Current		17.5		mA	
LO to RF Isolation	36			dB	
Mixer - GPS					
Gain	16.5	18.5	20.0	dB	
Noise Figure		7.5		dB	
Input IP3		-2.0		dBm	
Current		16.0		mA	
LO to RF Isolation	36			dB	
Mixer - IMT-2000					
Gain	11.5	13.5	15.0	dB	
Noise Figure		8.5		dB	
Input IP3		0.0		dBm	
Current		16.0		mA	
LO to RF Isolation	36			dB	
Other					
LO-IF Isolation	36			dB	
RF-IF Isolation	40			dB	
LNA Out to Mixer In Isolation	30	40		dB	
LO-LNA In Isolation, Any State	35			dB	
Control Lines					LNA GAIN, ENABLE, TX BUFF ENAB
Input Capacitance			1	pF	
Local Oscillator Input					IF = 183.6MHz/210.38MHz/220.38MHz
KPCS, US PCS, GPS, IMT-2000					
Input Power	-10	-4	0	dBm	
Input Frequency	1391		2360	MHz	
TX (Local Oscillator)					Single-ended 50Ω load
Buffer					
PCS					
Output Power	-11	-7		dBm	
Output Frequency	1600		2300	MHz	
Current Consumption		2		mA	

NOTE: Mixer performance can be changed with external IF load/tuning.

## LNA Performance versus Current (As a function of ISET1 Resistance)

Gain (dB)	IIP3 (dBm)	Noise Figure (dB)	ISET1 Resistance (k $\Omega$ )	Current (mA)
15.6	7.3	1.4	36	4.6
15.7	9.7	1.4	33	4.9
15.9	16.8	1.4	30	5.4
16.1	12.3	1.4	27	6.1
16.2	10.6	1.4	24	6.7
16.4	9.6	1.4	22	7.3
16.4	9.4	1.4	20	7.9

## Mixer Performance versus Current (As a function of ISET2 Resistance)

Gain (dB)	IIP3 (dBm)	Noise Figure (dB)	ISET2 Resistance (k $\Omega$ )	Current (mA)
14.2	4.0	6.7	6.8	25.6
14.2	3.7	6.6	7.5	24.6
14.1	3.5	6.5	8.3	23.9
14.0	2.9	6.4	9.1	22.8
13.8	2.6	6.4	10.0	22.2
13.8	2.4	6.3	11.0	21.8
13.5	1.8	6.3	12.0	20.7

## Evaluation Board Current Measurement

	ENABLE	LNA GAIN	TX BUFF ENAB	IDC (mA)
<b>US PCS Band</b>				
<b>Korean PCS Band</b>				
LNA On, TX Buffer Off	1	1	0	27.5
LNA Bypassed, TX Buffer Off	1	0	0	21.0
<b>GPS Band</b>				
LNA On, TX Buffer Off	1	1	0	24.5
LNA Bypassed, TX Buffer Off	1	0	0	18.5
<b>IMT-2000 Band</b>				
LNA On, TX Buffer Off	1	1	0	24.5
LNA Bypassed, TX Buffer Off	1	0	0	18.5

### NOTES:

All IDC current numbers include bias circuitry current of 1.5mA to 2.0mA (dependent on mode).

TX Buffer On: Add 2mA to total current.

## Cascaded Performance (Typical Values for $V_{CC}=2.75V$ )

**NOTE:** All total current numbers include bias circuitry current of 1.5mA to 2.0mA (dependent on mode).

Parameter	KPCS CDMA		PCS CDMA		GPS		IMT-2000	
	LNA ON	LNA OFF	LNA ON	LNA OFF	LNA ON	LNA OFF	LNA ON	LNA OFF
<b>Cascaded:</b>								
Gain (dB)	28.0	6.5	27.5	6.5	33.25	11.0	25.5	6.0
Noise Figure (dB)	1.8	14.5	2.0	14.5	1.7	15.0	2.5	16.0
Input IP3 (dBm)	-11.0	+10.0	-11.0	+10.0	-17.0	5.3	-12.0	+7.2
LO to IF Isolation (dB)	40	40	40	40	40	40	40	40
IF1 to RF Isolation (dB)	40	40	40	40	40	40	40	40
IF2 to RF Isolation (dB)	40	40	40	40	40	40	40	40
LO to LNA IN Isolation (dB)	40	40	40	40	40	40	40	40
Total Current (mA)	27.5	21.0	27.5	21.0	24.5	18.5	24.5	18.5

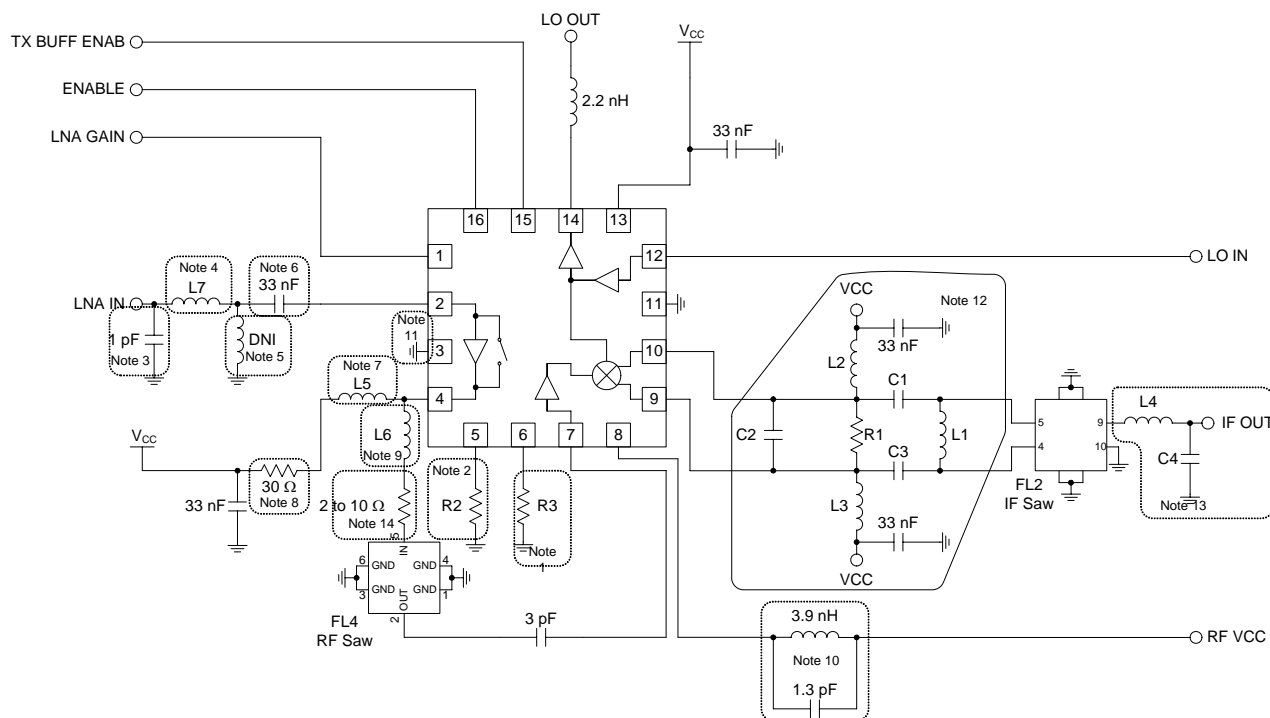
**NOTE:** Assumes 2.5dB image filter insertion loss. The TX Buffer is off.

Pin	Function	Type	Description	Interface Schematic
1	LNA GAIN	DI	Logic input. High activates LNA. Low selects LNA bypass mode.	
2	LNA IN	AI	US PCS LNA input. KPCS LNA input. GPS LNA input. IMT-2000 LNA input.	
3	GND	P	Ground via within 0.2mm of pin required.	
4	LNA OUT	AO	PCS LNA output. Simple external L-C components required for matching and VCC supply.	
5	ISSET2	AI	External resistor required to set the mixer operating current.	
6	ISSET1	AI	External resistor required to set the LNA operating current.	
7	MIX IN	AI	KPCS mixer RF single-end input. Matched to 50Ω. USPCS mixer RF single-end input. Matched to 50Ω. GPS mixer RF single-end input. Matched to 50Ω. IMT-2000 mixer RF single-end input. Matched to 50Ω.	
8	RF VCC	P	External capacitor and inductor placed close to package required.	
9	IF OUT+	AO	IF output. Open collector.	
10	IF OUT-	AO	IF output. Open collector.	See pin 9.
11	GND	P	Ground.	
12	LO IN	AI	LO single-end input. Matched to 50Ω.	
13	VCC	P	External bypass capacitor may be required.	
14	LO OUT	AO	LO output. Internal DC block. Drives 50Ω.	
15	TX BUFF ENAB	DI	Logic input. High enables TX LO output buffer amplifiers.	
16	ENABLE	DI	Logic input. Low level powers down the IC.	
Pkg Base	GND	P	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

## Legend:

DI=Digital Input from Baseband Chip  
 AI=Analog Input  
 AO=Analog Output  
 P=V<sub>CC</sub> or GND

## Application Schematic Differential IF Matching



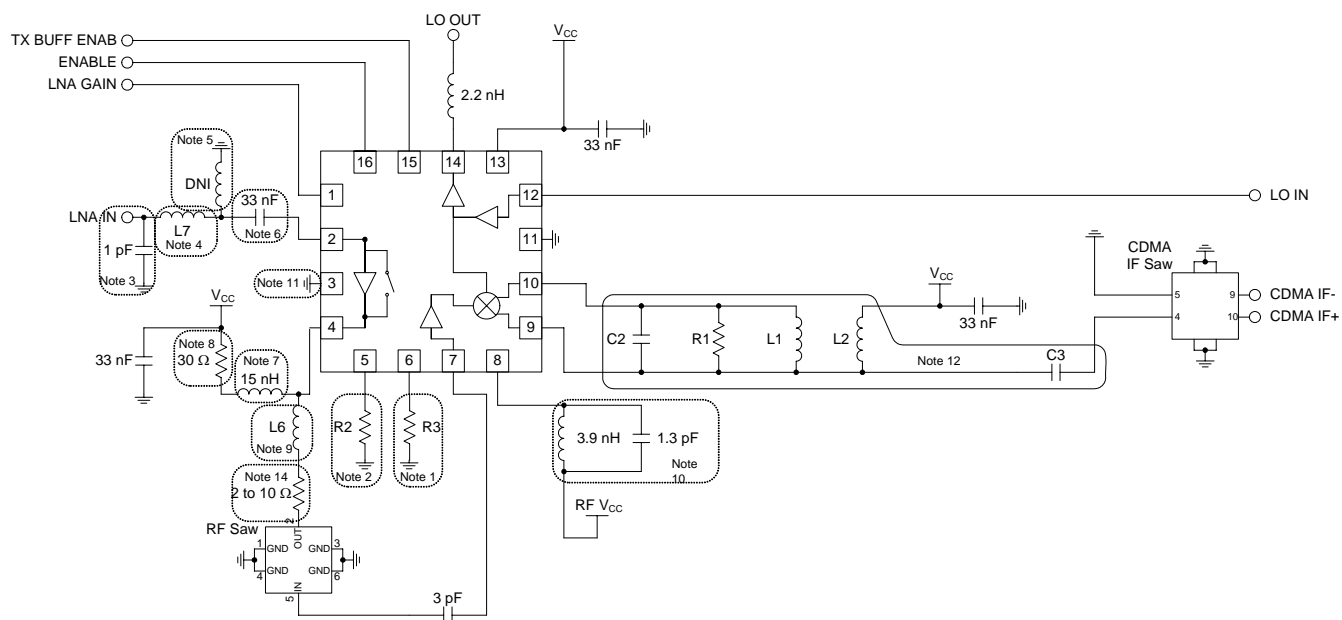
Application	C1 (pF)	C2 (pF)	C3 (pF)	C4 (pF)	L1 (nH)	L2 (nH)	L3 (nH)	L4 (nH)	L5 (nH)	L6 (nH)	L7 (nH)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)
US PCS, IF=184MHz	6.2	2.5	6.2	TBD	33	72	72	TBD	15	2.7	1.2	9.1	8.2	27.0
Korean PCS, IF=220MHz	5.1	3.0	5.1	TBD	33	50	50	TBD	15	3.3	1.5	7.5	8.2	27.0
GPS, IF=184MHz	3.9	1.5	3.9	TBD	33	110	110	TBD	18	4.7	1.5	DNI	13.0	27.0
IMT-2000, IF=190MHz	4.7	1.0	4.7	TBD	33	50	50	TBD	10	2.7	1.5	DNI	13.0	27.0

### NOTES:

1. This resistor sets the LNA current. Increasing the resistor value lowers the current.
2. This resistor sets the mixer current. Increasing the resistor value lowers the current.
3. This capacitor is used for optimum noise figure and input matching.
4. This inductor is used for optimum input match.
5. This inductor is used for optimum input match and IP3. Low impedance path to ground for optimum IP3.
6. DC-blocking capacitor. Not required with most SAW filters.
7. This inductor is used for LNA output match and as an RF choke.
8. This resistor is used to optimize performance over temperature and bias.
9. This inductor is used to optimize the LNA output match.
10. This inductor/capacitor parallel combination is used for mixer/preamp interstage matching and must be placed ~1.6mm or closer to pin 8.
11. Ground for LNA. Place ground via as close to pin as possible for maximum gain.
12. IF output matching component values are dependent on board layout, IF SAW filter, and the IF frequency selected. Please contact RFMD application engineering for assistance with IF output matching. See attached Single-Ended and Differential Tuning procedure.
13. These two values are contingent on type of IF SAW filter used.
14. Depending on SAW Filter used, resistor value will be between 2Ω to 10Ω.

## Application Schematic

### Single-End IF Matching



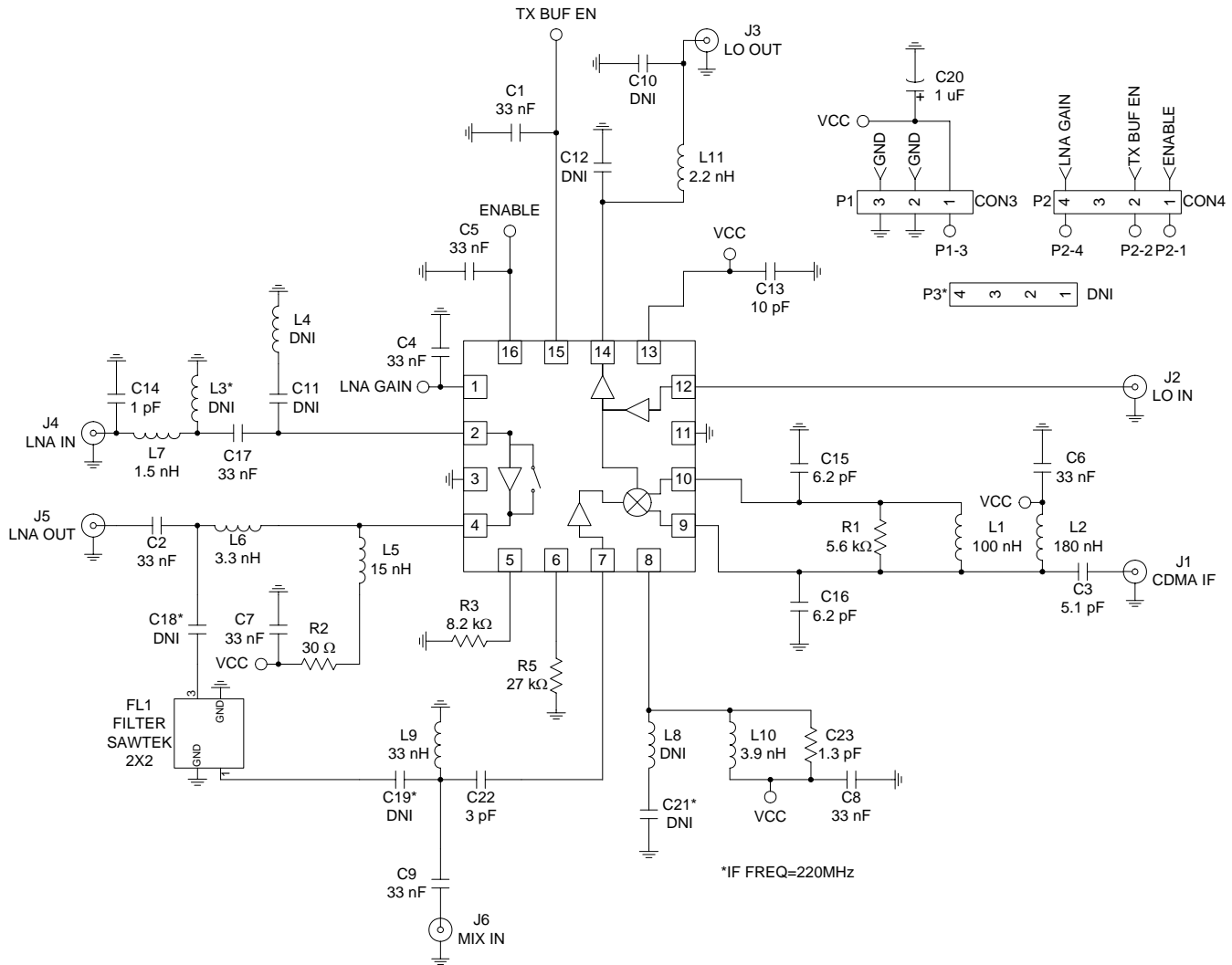
Application	C2 (pF)	C3 (pF)	L1 (nH)	L2 (nH)	L7 (nH)	L6 (nH)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)
US PCS, IF=184MHz	10.0	6.2	150	270	1.2	2.7	9.1	8.2	27.0
Korean PCS, IF=220MHz	12.0	5.1	100	180	1.5	3.3	7.5	8.2	27.0
GPS, IF=184MHz	6.0	3.9	220	270	1.5	4.7	DNI	13.0	27.0
IMT-2000, IF=190MHz	4.0	4.7	100	180	1.5	2.7	DNI	130	27.0

**NOTES:**

1. This resistor sets the LNA current. Increasing the resistor value lowers the current.
2. This resistor sets the mixer current. Increasing the resistor value lowers the current.
3. This capacitor is used for optimum noise figure and input matching.
4. This inductor is used for optimum input match.
5. This inductor is used for optimum input match and IP3. Low impedance path to ground for optimum IP3.
6. DC-blocking capacitor. Not required with most SAW filters.
7. This inductor is used for LNA output match and as an RF choke.
8. This resistor is used to optimize performance over temperature and bias.
9. This inductor is used to optimize the LNA output match.
10. This inductor/capacitor parallel combination is used for mixer/preamp interstage matching and must be placed ~1.6mm or closer to pin 8.
11. Ground for LNA. Place ground via as close to pin as possible for maximum gain.
12. IF output matching component values are dependent on board layout, IF SAW filter, and the IF frequency selected. Please contact RFMD application engineering for assistance with IF output matching. See attached Single-Ended and Differential Tuning procedure.
13. These two values are contingent on type of IF SAW filter used.
14. Depending on SAW Filter used, resistor value will be between  $2\Omega$  to  $10\Omega$ .

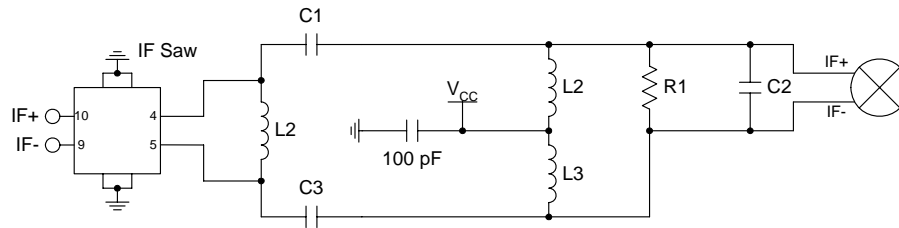
## Evaluation Board Schematic KPCS, IF = 220.38MHz

(Download [Bill of Materials](http://www.rfmd.com) from [www.rfmd.com](http://www.rfmd.com).)





## Differential IF Matching

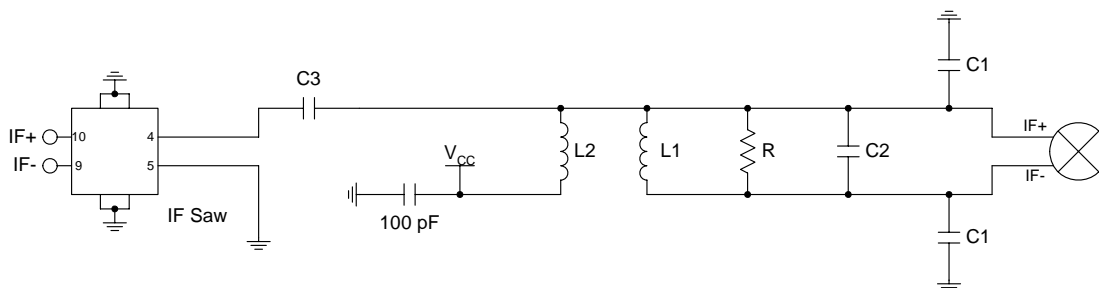


L2, L3 and C2 are chosen to resonate at the desired IF frequency. C2 can be omitted and the value of L1 increased and utilized solely as a choke to provide  $V_{CC}$  to the open-collector outputs, but it is strongly recommended that at least some small-valued C2 (a few pF) be retained for better mixer linearity performance. R1 is normally selected to match the input impedance of the IF filter. However, mixer performance can be modified by selecting an R value that is different from the IF filter input impedance, and inserting a conjugate matching network between the Resistive Output Network and the IF filter.

C1 and C3 serve dual purposes. C1 and C3 serve as a series DC block when a DC path to ground is present in the IF filter. In addition, C1 may be chosen to improve the combine performance of the mixer and IF filter. L1 should choose to resonate with the internal capacitance of the SAW filter. Usually, SAW filter has some capacitance. Otherwise, L1 could be eliminated.

A practical approach to obtain the differential matching is to tune the mixer to the correct load point for gain, IIP3, and NF using the single-end current combiner method. Second, use the component values found in the single-end approach as starting point for the differential matching. The two-shunt capacitors in the single-end matching could be converted to a parallel capacitor and the parallel inductor in the single-end matching needs to be converted in to a choke inductor. Third, set the DC block capacitors (C1 and C3) in the differential-end matching to a high value (i.e., 100pF) and retune the resonate circuit (C2, L2 and L3) and the resistor (R) for optimal performance. After optimal performance is achieved and if performance is not satisfactory, decrease the series capacitors until optimal performance is achieved.

## Single-End IF Matching



L1, C1, C2, and R form a current combiner which performs a differential to single-ended conversion at the IF frequency and sets the output impedance. In most cases, the resonance frequency is independent of R and can be set according to the following equation:

$$f_{IF} = \frac{1}{2\pi\sqrt{\frac{L1}{2}(C_1 + 2C_2 + C_{EQ})}}$$

Where  $C_{EQ}$  is the equivalent stray capacitance and capacitance looking into pins 9 and 10. An average value to use for  $C_{EQ}$  is 2.5pF.

R can then be used to set the output impedance according to the following equation:

$$R = \left( \frac{1}{4 \cdot R_{OUT}} - \frac{1}{R_P} \right)^{-1}$$

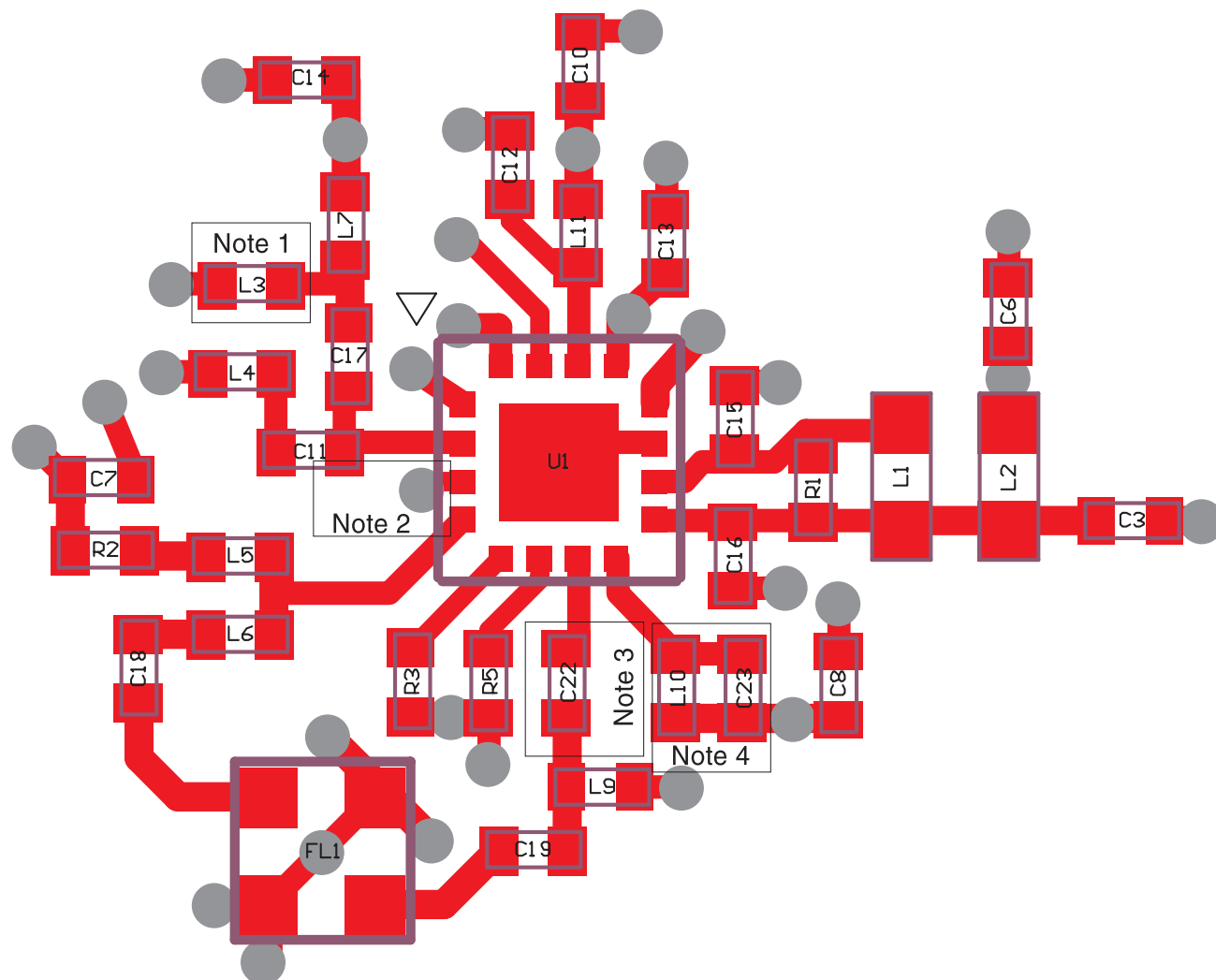
where  $R_{OUT}$  is the desired output impedance and  $R_P$  is the parasitic equivalent parallel resistance of L1.

$C_2$  should first be set to 0 and C1 should be chosen as high as possible (not greater than 39pF), while maintaining an  $R_P$  of L1 that allows for the desired  $R_{OUT}$ . If the self-resonant frequencies of the selected C1 produce unsatisfactory linearity performance, their values may be reduced and compensated for by including C2 capacitor with a value chosen to maintain the desired  $F_{IF}$  frequency.

L2 and C3 serve dual purposes. L2 serves as an output bias choke, and C3 serves as a series DC block.

In addition, L2 and C3 may be chosen to form an impedance matching network if the input impedance of the IF filter is not equal to  $R_{OUT}$ . Otherwise, L2 is chosen to be large (suggested 120nH) and C3 is chosen to be large (suggested 22nF) if a DC path to ground is present in the IF filter, or omitted if the filter is DC-blocked.

## RF2860 Layout Requirements



### NOTES:

1. This component is not required on the evaluation board. It may be required on the phone board for optimum IIP3. Component placeholder should be on phone board.
2. Ground for LNA emitter. For maximum gain, place ground via as close to pin 3 as possible.
3. This capacitor is required as part of the mixer input match.
4. This inductor/capacitor parallel combination is used for mixer/preamplifier interstage tuning. It must be placed ~1.6mm or closer to pin 8.

## PCB Design Requirements

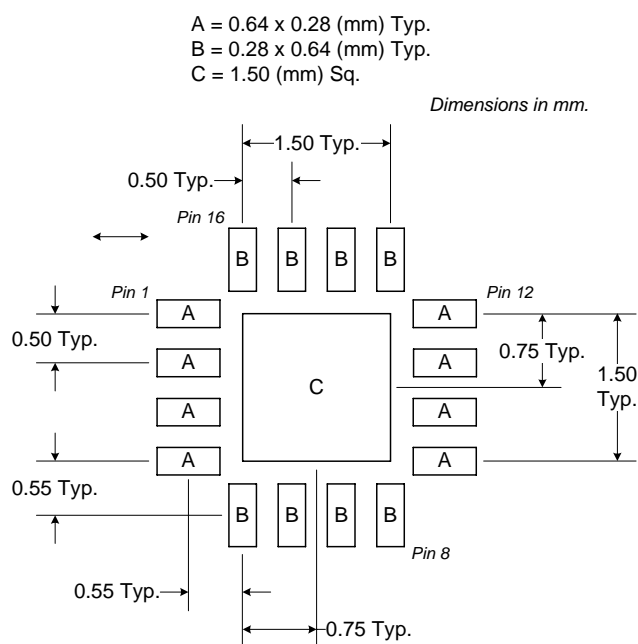
### PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

### PCB Land Pattern Recommendation

PCB land patterns for PFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

### PCB Metal Land Pattern



**Figure 1. PCB Metal Land Pattern (Top View)**

## Tape and Reel Information

Carrier tape basic dimensions are based on EIA481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

Carrier tape is wound or placed onto a shipping reel either 330 mm (13 inches) in diameter or 178 mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier, ESD bag, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125°C. If baking is required, devices may be baked according to section 4, table 4-1, column 8 of Joint Industry Standard IPC/JEDEC J-STD-033A.

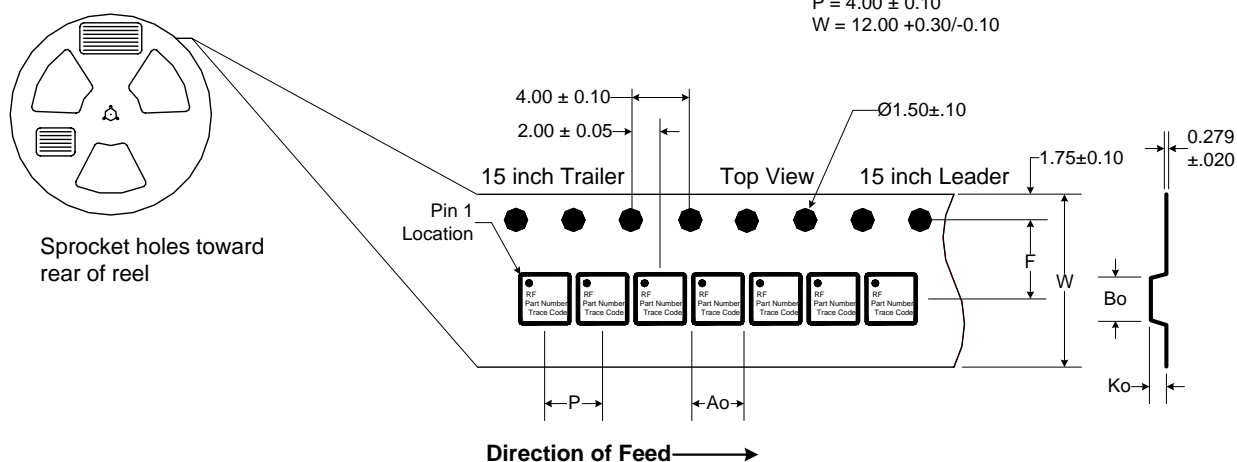
The following table provides useful information for carrier tape and reels used for shipping the devices described in this document.

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF2860TR7	7 (178)	2.4 (61)	12	4	Single	2500

### QFN (Carrier Tape Drawing with Part Orientation)

Notes:

1. All dimensions are in millimeters (mm).
2. Unless otherwise specified, all dimension tolerances per EIA-481.



**RF2860**