Preliminary **RF2192**

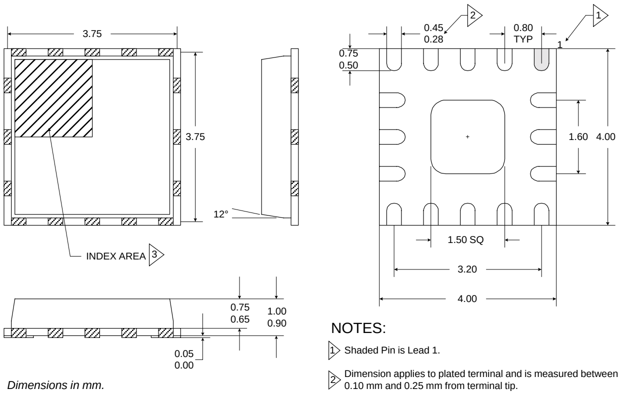
3V 900MHZ LINEAR POWER AMPLIFIER

Typical Applications

- 3V CDMA/AMPS Cellular Handsets
- 3V JCDMA Cellular Handsets
- 3V CDMA2000 Cellular Handsets
- 3V TDMA/GAIT Cellular Handsets
- Spread-Spectrum Systems
- Portable Battery-Powered Equipment

Product Description

The RF2192 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA/AMPS and CDMA2000 hand-held digital cellular equipment, spread-spectrum systems, and other applications in the 800MHz to 960MHz band. The RF2192 has a low power mode to extend battery life under low output power conditions. The device is packaged in a 16 pin, 4mmx4mm leadless chip carrier.



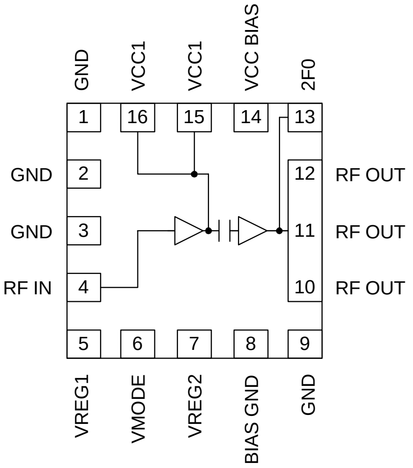
NOTES:

1. Shaded Pin is Lead 1.
2. Dimension applies to plated terminal and is measured between 0.10 mm and 0.25 mm from terminal tip.
3. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The identifier may be either a mold or marked feature.
4. Pins 1 and 9 are fused.
5. Package Warpage: 0.05 max.

Package Style: LCC, 16-Pin, 4x4

Optimum Technology Matching® Applied

☐ Si BJT ☑ GaAs HBT ☐ GaAs MESFET
☐ Si Bi-CMOS ☐ SiGe HBT ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V Supply
- 29dBm Linear Output Power
- 37% Linear Efficiency
- Low Power Mode
- 45 mA idle current
- 47% Peak Efficiency 31dBm Output

Ordering Information

RF2192	3V 900MHz Linear Power Amplifier
RF2192 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

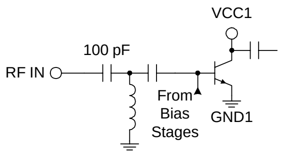
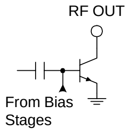
Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage ($P_{OUT}\leq$31dBm)	+5.2	V_{DC}
Mode Voltage (V_{MODE})	+4.2	V_{DC}
Control Voltage (V_{REG})	+3.0	V_{DC}
Input RF Power	+10	dBm
Operating Case Temperature	-30 to +110	°C
Storage Temperature	-30 to +150	°C
Moisture Sensitivity	Modified JEDEC Level 2	

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power State (V_{MODE} Low)					Case T=25°C, V_{CC}=3.4V, V_{REG}= 2.85V, V_{MODE}=0V to 0.5V, Freq=824MHz to 849MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Linear Gain	27	30		dB	
Second Harmonic		-33		dBc	
Third Harmonic		<-60		dBc	
Maximum Linear Output Power (CDMA Modulation)	29			dBm	
Total Linear Efficiency		37		%	P_{OUT}=29dBm
Adjacent Channel Power Rejection		-48	-44	dBc	ACPR@885kHz
		-58	-56	dBc	ACPR@1980kHz
Input VSWR		2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc
Noise Power		-136		dBm/Hz	At 45MHz offset with alternative tune. See schematic.
Low Power State (V_{MODE} High)					Case T=25°C, V_{CC}=3.4V, V_{REG}=2.85V, V_{MODE}=1.8V to 3V, Freq=824MHz to 849MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Linear Gain	19	22		dB	
Second Harmonic		-33		dBc	
Third Harmonic		<-60		dBc	
Maximum Linear Output Power (CDMA Modulation)	16	20		dBm	
Max I_{CC}		150		mA	P_{OUT}=+16dBm (all currents included)
Adjacent Channel Power Rejection		-48	-46	dBc	ACPR@885kHz
		<-60	-58	dBc	ACPR@1980kHz
Input VSWR		2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc

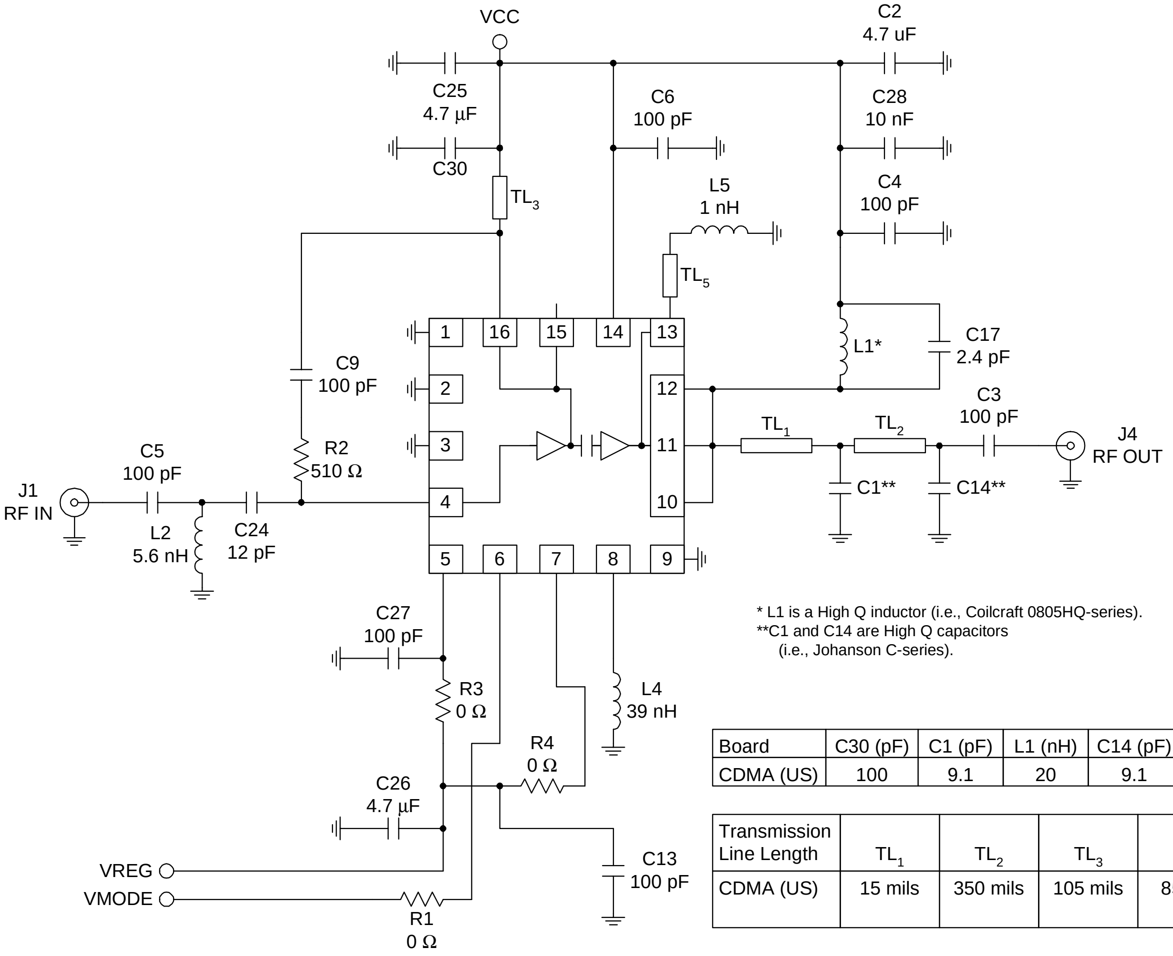
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power State CDMA 2000 1x (V_{MODE} LOW)					Case T=25^{o}C, V_{CC}=3.4V, V_{REG}=2.85V. V_{MODE}=0V to 0.5V, Freq=824MHz to 849MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Linear Gain		29		dB	
Pilot+DCCH 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	26.5			dBm	2.5dB Backoff included in IS95D CCDF 1% 5.4dB Peak Average Ratio at CCDF 1%
Adjacent Channel Power Rejection		-47		dBc	ACPR@88.5kHz
		<-60		dBc	ACPR@1.98MHz
Pilot+FCH 9800+SCHO 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	29			dBm	4.5dB Peak Average Ratio at CCDF 1%
Adjacent Channel Power Rejection		-47		dBc	ACPR@885kHz
		<-60		dBc	ACPR@1.98MHz
Low Power State CDMA 2000 1x (V_{MODE} HIGH)					Case T=25^{o}C, V_{CC}=3.4V, V_{REG}=2.85V. V_{MODE}=1.8V to 3V, Freq=824MHz to 849MHz
Frequency Range	824		849	MHz	
Linear Gain		22		dB	
Pilot+DCCH 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	16	20		dBm	5.4dB Peak to Average Ratio at CCDF 1%
Adjacent Channel Power Rejection		-48		dBc	ACPR@885kHz
		<-85		dBc	ACPR@1.98MHz
Efficiency		15		%	P_{OUT}=20dBm
Pilot+FCH 9600+SCHO 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	16	20		dBm	4.5dB Peak to Average Ratio at CCDF 1%
Adjacent Channel Power Rejection		<-50		dBc	ACPR@885kHz
		<-65		dBc	ACPR@1.98MHz
FM Mode					Case T=25°C, V_{CC}=3.4V, V_{REG}=2.85V, V_{MODE}=0V to 0.5V, Freq=824MHz to 849MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Gain		30		dB	
Second Harmonic		-33		dBc	
Third Harmonic		<-60		dBc	
Max CW Output Power	31	32		dBm	
Total Efficiency (AMPS mode)		47		%	P_{OUT}=31dBm (room temperature)
Input VSWR		2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DC Supply					
Supply Voltage	3.0	3.4	4.2	V	The maximum power out for V_{CC}=3.0V is 28dBm.
Quiescent Current		160		mA	V_{MODE}=Low
		45	70	mA	V_{MODE}=High
V_{REG} Current			10	mA	
V_{MODE} Current			1	mA	
Turn On/Off Time			<40	µs	Time between V_{REG} turned on and PA reaching full power. Turn on/off time can be reduced by lowering the bypass capacitor value on the V_{REG} line.
Total Current (Power Down)			10	µA	V_{REG}=Low
V_{REG} "Low" Voltage	0		0.5	V	
V_{REG} "High" Voltage	2.75	2.85	2.95	V	
V_{MODE} "Low" Voltage	0		0.5	V	
V_{MODE} "High" Voltage	1.8	2.85	3.0	V	

Pin	Function	Description	Interface Schematic
1	**GND**	Ground connection.	
2	**GND**	Ground connection.	
3	**GND**	Ground connection.	
4	**RF IN**	RF input. An external 100pF series capacitor is required as a DC block. In addition, shunt inductor and series capacitor are required to provide 2:1VSWR.	
5	**VREG1**	Power Down control for first stage. Regulated voltage supply for amplifier bias. In Power Down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
6	**VMODE**	For nominal operation (High Power Mode), V_{MODE} is set LOW. When set HIGH, the driver and final stage are dynamically scaled to reduce the device size and as a result to reduce the idle current.	
7	**VREG2**	Power Down control for the second stage. Regulated voltage supply for amplifier bias. In Power Down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
8	**BIAS GND**	Bias circuitry ground. See application schematic.	
9	**GND**	Ground connection.	
10	**RF OUT**	RF output and power supply for final stage. This is the unmatched collector output of the second stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 824MHz to 849MHz. It is important to select an inductor with very low DC resistance with a 1A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
11	**RF OUT**	Same as pin 10.	See pin 10.
12	**RF OUT**	Same as pin 10.	
13	**2FO**	Harmonic trap. This pin connects to the RF output but is used for providing a low impedance to the second harmonic of the operating frequency. An inductor or transmission line resonating with an on chip capacitor at 2fo is required at this pin.	
14	**VCC BIAS**	Power supply for bias circuitry. A 100pF high frequency bypass capacitor is recommended.	
15	**VCC1**	Power supply for first stage.	
16	**VCC1**	Same as Pin 15.	
Pkg Base	**GND**	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Evaluation Board Schematic
US - CDMA

(Download Bill of Materials from www.rfmd.com.)



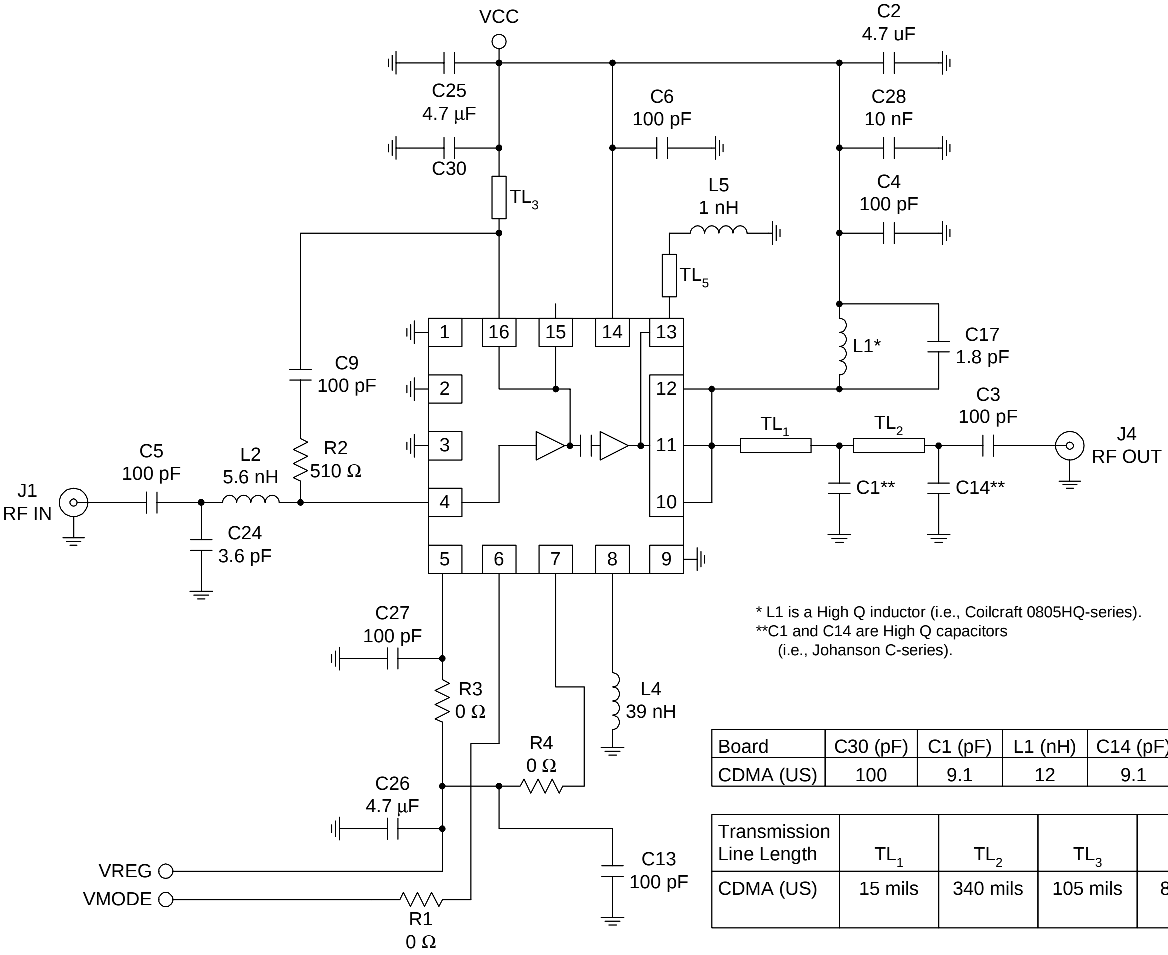
* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).
**C1 and C14 are High Q capacitors
(i.e., Johanson C-series).

Board	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (US)	100	9.1	20	9.1

Transmission Line Length	TL_1	TL_2	TL_3	TL_5
CDMA (US)	15 mils	350 mils	105 mils	85 mils

Evaluation Board Schematic
US - CDMA Alternative Tune

(Download Bill of Materials from www.rfmd.com.)



* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).
**C1 and C14 are High Q capacitors
(i.e., Johanson C-series).

Board	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (US)	100	9.1	12	9.1

Transmission Line Length	TL_1	TL_2	TL_3	TL_5
CDMA (US)	15 mils	340 mils	105 mils	85 mils

Evaluation Board Layout

2.0” x 2.0”

Board Thickness 0.031”, Board Material FR-4, Multi-Layer, Ground Plane at 0.015”