





RELEASE Ø DATA SHEET

FEATURES

- Two Selectable Gain Modes
- Gain Flatness as Low as 0.5 dB Over 400 MHz Tuning Bands
- Excellent Linearity Performance Over Wide Bandwidths
- 3.3 V and 5 V Supply Voltages
- Flexible Biasing Provides Latitude for Linearity Optimization
- 100 mA Native Mode Quiescent Current Consumption
- 50 Ω Single-ended Input and Output Impedances
- -40 to 115 °C Operating Temperature Range
- Compact 3 x 3 mm QFN-16 Package
- Process: GaAs pHEMT
- RoHS Compliant

Reference: High Gain Mode / 5 V / 100 mA / 3.55 GHz

Gain: 37.5 dBOP1dB: 24.6 dBmOIP3: 31.1 dBmNoise Figure: 1.9 dB

Reference: Low Gain Mode / 5 V / 100 mA / 3.55 GHz

Gain: 31.1 dBOP1dB: 24 dBmOIP3: 31.4 dBmNoise Figure: 1.9 dB

APPLICATIONS

- Linear Driver / Pre-Driver Amplifiers
- 5G Sub-6 GHz Massive MIMO Base Stations
- Small Cells and Cellular Repeaters
- Millimeter Wave IF Stages
- High Performance RF Infrastructure

ORDERING INFORMATION Buy it Now

M DESCRIPTION

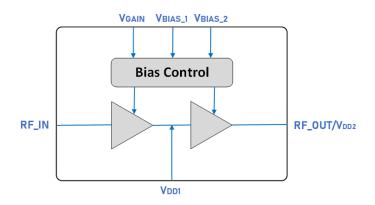
The GRF5126 is a high-gain, two-stage driver amplifier targeting 3.3 to 3.8 GHz wireless infrastructure applications. Custom tuning allows the device to work from 1.8 to 5 GHz. The device delivers 24.6 dBm of OP1dB, 31.1 dBm of OIP3 and a low Noise Figure (NF) of 1.9 dB. The device also provides two selectable gain modes allowing a single component to address multiple use cases.

For optimal efficiency and linearity, the amplifier was designed to operate with a single 5 V supply voltage while using only 85-100 mA of quiescent current. 3.3 V supplies can also be used while still yielding 21 dBm of OP1dB. If desired, IDDQ can be increased beyond the native biasing point for enhanced linearity performance.

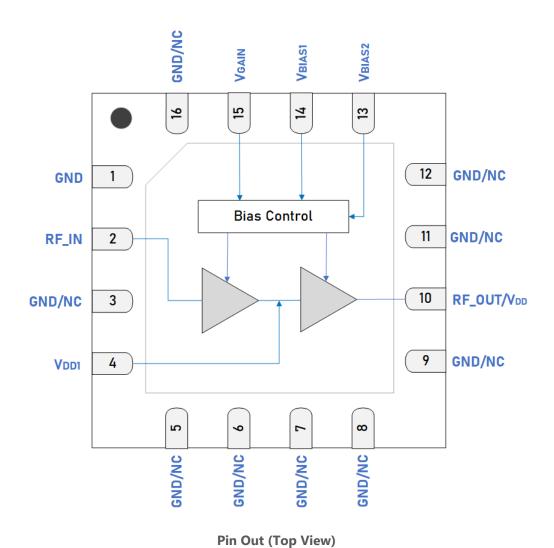
The GRF5126 is designed for $50~\Omega$ systems, typically needing only a two-element shunt-series match on the input and output ports. Separate tunes allow the GRF5126 to maintain its excellent performance over bandwidths exceeding 400 MHz.

Additional tunes can be found on the GRF5126 "Custom Tunes" product page: <u>GRF5126 Custom Tunes</u>

M BLOCK DIAGRAM











Pin Assignments

Pin	Name	Description	Note
1	GND	Ground	Internally grounded. This pin must be grounded with a via as close to the pin as possible.
2	RF_IN	RF Input	An external DC blocking capacitor must be used.
3, 5, 6, 7, 8, 9, 11, 12, 16	GND/NC	Ground or No Connect	No internal connection to die. These pins can be left unconnected, or can be connected to ground (recommended). Use a via as close to the pin as possible if grounded.
4	V _{DD1}	V _{DD} Bias Voltage	Pull up to V_{DD} through inductor and use bypass capacitors as close to the pin as possible. In addition to supplying the device with a DC voltage, there is also an RF signal present.
10	RF_OUT/V _{DD}	OUT/V _{DD} RF Output V _{DD} must be applied through a ch	
13	V _{BIAS2}	Second Stage Bias Set	Connect via resistor to a common V_{DD} . V_{BIAS2} and series resistor sets I_{DDQ2} . Setting $V_{BIAS2} < 0.2 \text{ V}$ will disable Stage 2 of the device.
14	V _{BIAS1}	First Stage Bias Set	Connect via resistor to a common V_{DD} . V_{BIAS1} and series resistor sets I_{DDQ1} . Setting $V_{BIAS1} < 0.2 \text{ V}$ will disable Stage 1 of the device.
15	V _{GAIN}	Gain Select Voltage	Set $V_{GAIN} \ge 1.0$ to 2.5 V for High Gain Mode, and $V_{GAIN} \le 0.5$ V for Low Gain Mode.
PKG BASE	GND	Ground	Provides DC and RF ground for the amplifier, as well as thermal heat sink. In order to match the devices rated performance, it is strongly recommended to use multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on the schematic page.





Absolute Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V _{DD}	0	6	V
RF Input Power: Load VSWR, 2:1; V _{DD} < 6 V	P _{IN MAX}		23	dBm
Operating Temperature (Package Base)	T _{PKG BASE}	-40	115	°C
Maximum Channel Temperature (MTTF > 106 hours)	T _{MAX}		170	°C
Maximum Dissipated Power (Stage 1)	P _{DISS MAX}		185	mW
Maximum Dissipated Power (Stage 2)	P _{DISS MAX}		475	mW

Electrostatic Discharge

Charged Device Model	CDM	750	kV
Human Body Model	НВМ	250	V

Storage

Storage Temperature	T _{STG}	-65	150	°C
Moisture Sensitivity Level	MSL		1	



Caution! ESD Sensitive Device.

Exceeding Absolute Maximum Rating conditions may cause permanent damage.

Note: For additional information, please refer to Manufacturing Note MN-001 - Packaging and Manufacturing Information.



All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging. For additional information, please refer to the Certificate of RoHS Compliance.





Recommended Operating Conditions

Parameter	Symphol	Specification			Unit	Condition
Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
Supply Voltage	V _{DD}	3	5	5.5	V	
Operating Temperature Range	T _{PKG BASE}	-40		115	°C	Measured on package base.
		1.8		2.2		2 GHz tuning set.
		2.3		2.7		2.5 GHz tuning set.
RF Frequency Range (note 1 & 2)	F _{RF}	3.3		3.8	GHz	3.55 GHz tuning set.
		3.8		4.2		4 GHz tuning set.
		4.4		5		4.7 GHz tuning set.
RF_IN Port Impedance	Z _{RFIN}		50		Ω	Single ended, with respective matching elements from each tuning set.
RF_OUT Port Impedance	Z _{RFOUT}		50		Ω	Single ended, with respective matching elements from each tuning set.

Note 1: Operation outside of this range is supported by using different custom tunes. Examples of other optimized tunes can be found here: <u>GRF5126 Custom Tunes</u>

Note 2: Contact the Guerrilla RF Applications team for guidance on optimizing the tuning of the device for alternative bands.



Nominal Operating Parameters - General

Davamatav	Cymphol	S	pecificatio	n	Unit	Condition	
Parameter	Symbol	Min.	Тур.	Max.	Unit		
V _{BIAS1} Logic Input Low	V _{IL}	0		0.2	V	R_{BIAS1} = 3.24 kΩ, Measured at V_{BIAS1} node (with bias-setting	
V _{BIAS1} Logic Input High	V _{IH}	1.5	5	V _{DD}	V	resistor in line between node and pin 14).	
V _{BIAS2} Logic Input Low	V _{IL}	0		0.2	V	$R_{BIAS2} = 2.7 \text{ k}\Omega$, Measured at V_{BIAS2} node (with bias-setting	
V _{BIAS2} Logic Input High	V _{IH}	1.5	5	V _{DD}	V	resistor in line between node and pin 13).	
VGAIN Logic Input Low	V _{IL}	0		0.5	V	Managered at V made	
VGAIN Logic Input High	V _{IH}	1.0	1.8	2.5	V	Measured at V _{GAIN} node.	
V _{BIAS1} Logic High Current	I _{IH}		1.1		mA	$V_{BIAS1} = 5 V.$	
V _{BIAS1} Logic Low Current	I _{IL}		400		nA	$V_{BIAS1} = 0.2 \text{ V}.$	
V _{BIAS2} Logic High Current	I _{IH}		1.5		mA	$V_{BIAS2} = 5 V.$	
V _{BIAS2} Logic Low Current	I _{IL}		55		μΑ	$V_{BIAS2} = 0.2 \text{ V}.$	
VGAIN Logic High Current	I _{IH}		10		μΑ	V _{GAIN} = 1.8 V.	
VGAIN Logic Low Current	I _{IL}		20		nA	V _{GAIN} = 0.5 V.	
STBY Switching Rise Time	t _{STBY-RISE}		200		ns	Turn ON time: V _{BIAS1} & V _{BIAS2} LOW to HIGH (note 3).	
STBY Switching Fall Time	t _{STBY-FALL}		50		ns	Turn OFF time: V _{BIAS1} & V _{BIAS2} HIGH to LOW (note 4).	
GAIN SEL Switching Rise Time	t _{GAIN-SEL-RISE}		200		ns	Low to High Gain mode (note 5).	
GAIN SEL Switching Fall Time	t _{GAIN-SEL-FALL}		50		ns	High to Low Gain mode (note 6).	

Disabled Mode

Standby Current	I _{STBY}	800		μΑ	$V_{DD} = 5 \text{ V}, V_{GAIN} = V_{BIAS1} = V_{BIAS2} = 0 \text{ V}.$
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Note 3: Switching Time: 50% of V_{BIAS} to 90% of P_{OUT} . **Note 4:** Switching Time: 50% of V_{BIAS} to 10% of P_{OUT} . **Note 5:** Switching Time: 50% of V_{GAIN} to 90% of P_{OUT} . **Note 6:** Switching Time: 50% of V_{GAIN} to 10% of P_{OUT} .



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Thermal Data

Parameter	Symbol	Symbol Symbol				Condition	
		Min.	Тур.	Max.		001141141011	
Thermal Resistance (Infrared Scan) Stage 1	Θ _{JC}		228		°C/W	On standard evaluation board.	
Thermal Resistance (Infrared Scan) Stage 2	Θ _{JC}		94		°C/W	On standard evaluation board.	
Channel Temperature @ 115 °C Reference (Package Heat Sink)	T _{CHANNEL}		148		°C	V _{DD} : 5.0 V, I _{DDQ} : 100 mA, P _{DISS:} 500 mW, No RF (note 6).	

Note 6: MTTF > 10^6 hours for $T_{CHANNEL} \le 170$ °C.



Nominal Operating Parameters - RF High Gain Configuration

The following conditions apply unless noted otherwise: typical application schematic using the 3.3 to 3.8 GHz tuning set, $R_{BIAS1} = 3.24 \text{ k}\Omega$, $R_{BIAS2} = 2.7 \text{ k}\Omega$, $V_{DD} = 5 \text{ V}$, $V_{GAIN} = 1.8 \text{ V}$ (High Gain Mode), 50 Ω system impedance, $P_{OUT} = 4 \text{ dBm}$, $F_{TEST} = 3.55 \text{ GHz}$, $T_{PKG BASE} = 25 ^{\circ}\text{C}$. Evaluation board losses are included within the specifications.

		:	Specificatio	n			
Parameter	Symbol	Min.	Тур. Мах.		Unit	Condition	
Supply Quiescent Current	I _{DDQ}		97		mA		
Supply Current with RF Applied	I _{DD}		100		mA	P _{OUT} = 14 dBm.	
Gain	S21		37.5		dB	F _{RF} = 3.55 GHz. Pin = -25 dBm.	
Gain Flatness	S21 _{FLAT}		1.6		dB	F _{RF} = 3.3 to 3.8 GHz. Pin = -25 dBm.	
Gain Variation Over Temp	S21 _{TEMP}		+1.1/-1.9		dB	$T_{PKG\ BASE}$ = -40 to 115 °C, referenced to $T_{PKG\ BASE}$ = 25 °C.	
Standby Mode Gain	S21 _{STBY}		-37		dB	V _{BIAS1} < 0.2 V, V _{BIAS2} < 0.2 V. Pin = 10 dBm.	
Input Return Loss	S11		-15		dB	F _{RF} = 3.3 to 3.8 GHz.	
Output Return Loss	S22		-15		dB	F _{RF} = 3.3 to 3.8 GHz.	
Reverse Isolation	S12		-50		dB	F _{RF} = 3.3 to 3.8 GHz.	
Evaluation Board Noise Figure	NF		1.9		dB		
Output 3rd Order Intercept	OIP3		31.1		-ID	4 dBm P _{OUT} per tone at 2 MHz spacing, V _{DD} = 5 V, T _{PKG BASE} = 25 °C.	
Point	OIP3 _{HOT}		29.2		- dBm	4 dBm P _{OUT} per tone at 2 MHz spacing, V _{DD} = 5 V T _{PKG BASE} = 115 °C.	
Output 1 dB Compression	OP1dB		24.6		dBm	V_{DD} = 5 V, $T_{PKG BASE}$ = 25 °C.	
Power	OP1dB _{HOT}	OP1dB _{HOT}		23.2		V _{DD} = 5 V, T _{PKG BASE} = 115 °C.	



Nominal Operating Parameters - RF

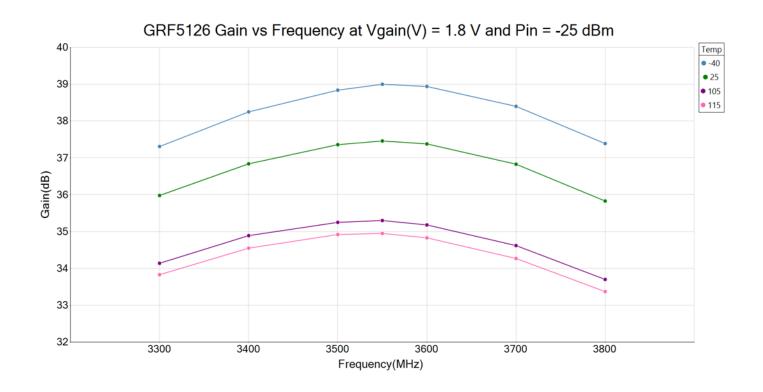
Low Gain Configuration

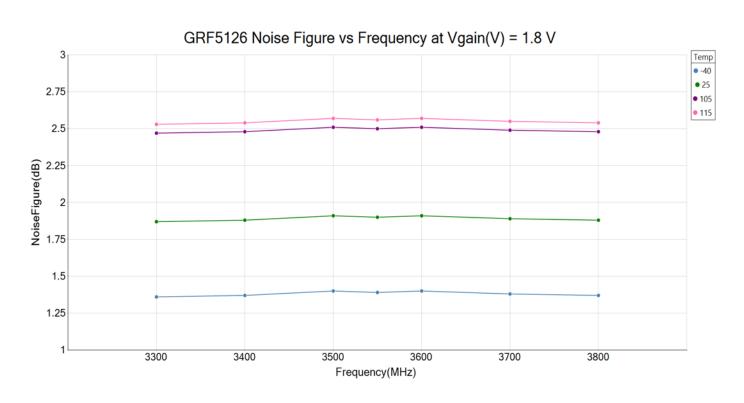
The following conditions apply unless noted otherwise: typical application schematic using the 3.3 to 3.8 GHz tuning set, $R_{BIAS1} = 3.24 \text{ k}\Omega$, $R_{BIAS2} = 2.7 \text{ k}\Omega$, $V_{DD} = 5 \text{ V}$, $V_{GAIN} = 0 \text{ V}$ (Low Gain Mode), 50 Ω system impedance, $P_{OUT} = 4 \text{ dBm}$, $F_{TEST} = 3.55 \text{ GHz}$, $T_{PKG BASE} = 25 ^{\circ}\text{C}$. Evaluation board losses are included within the specifications.

Downwater	Consolo a l	9	Specification		Unit	Condition	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition	
Supply Quiescent Current	I _{DDQ}		97		mA		
Supply Current with RF Applied	I _{DD}		100		mA	P _{OUT} = 14 dBm.	
Gain	S21		31.1		dB	F _{RF} = 3.55 GHz. Pin = -25 dBm.	
Gain Flatness	S21 _{FLAT}		0.65		dB	F _{RF} = 3.3 to 3.8 GHz. Pin = -25 dBm.	
Gain Variation Over Temp	S21 _{TEMP}		+1.1/-1.9		dB	$T_{PKG\ BASE}$ = -40 to 115 °C, referenced to $T_{PKG\ BASE}$ = 25 °C.	
Standby Mode Gain	S21 _{STBY}		-37		dB	B $V_{BIAS1} < 0.2 \text{ V}, V_{BIAS2} < 0.2 \text{ V}.$ Pin = 10 dBm.	
Input Return Loss	S11		-15		dB	F _{RF} = 3.3 to 3.8 GHz.	
Output Return Loss	S22		-8		dB	F _{RF} = 3.3 to 3.8 GHz.	
Reverse Isolation	S12		-50		dB	F _{RF} = 3.3 to 3.8 GHz.	
Evaluation Board Noise Figure	NF		1.9		dB		
Output 3rd Order Intercept	OIP3		31.4		dD.se	4 dBm P_{OUT} per tone at 2 MHz spacing, $V_{DD} = 5 V$, $T_{PKG \; BASE} = 25 \; ^{\circ}C$.	
Point	OIP3 _{HOT}		29.3		dBm	4 dBm P_{OUT} per tone at 2 MHz spacing, $V_{DD} = 5 V$, $T_{PKG BASE} = 115 ^{\circ}C$.	
Output 1 dB Compression	OP1dB		24		dBm	$V_{DD} = 5 \text{ V}, T_{PKG \text{ BASE}} = 25 \text{ °C}.$	
Power	OP1dB _{HOT}		22.1		UDIII	V _{DD} = 5 V, T _{PKG BASE} = 115 °C.	



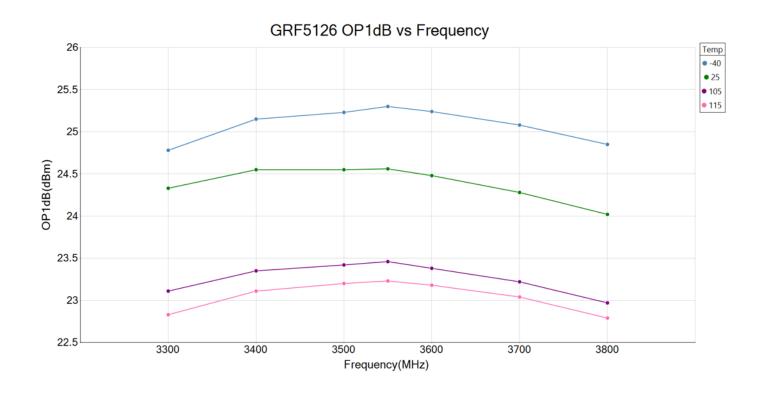
Typical Operating Curves: 3.3 to 3.8 GHz Tune, $V_{DD} = 5 \text{ V}$







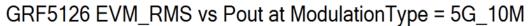
Typical Operating Curves: 3.3 to 3.8 GHz Tune, $V_{DD} = 5 \text{ V}$

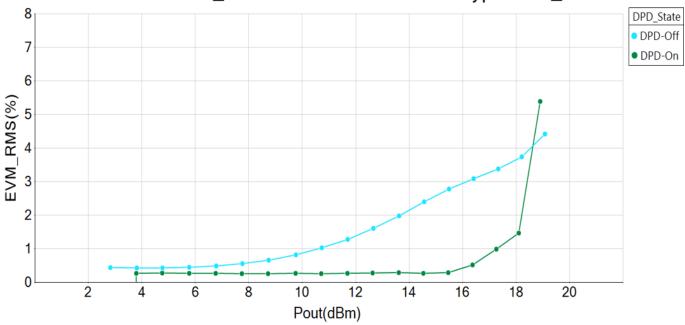




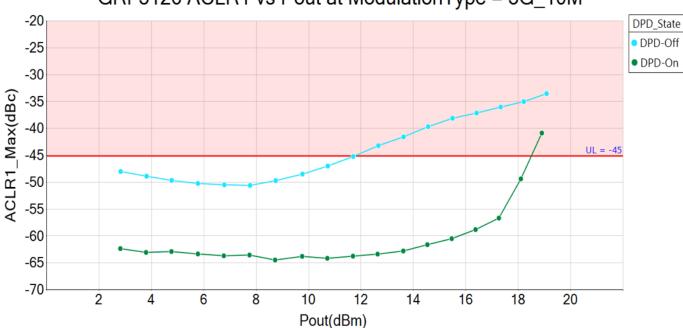


Typical Operating Curves: 3.3 to 3.8 GHz Tune, $V_{DD} = 5 \text{ V}$, $F_{RF} = 3550 \text{ MHz}$





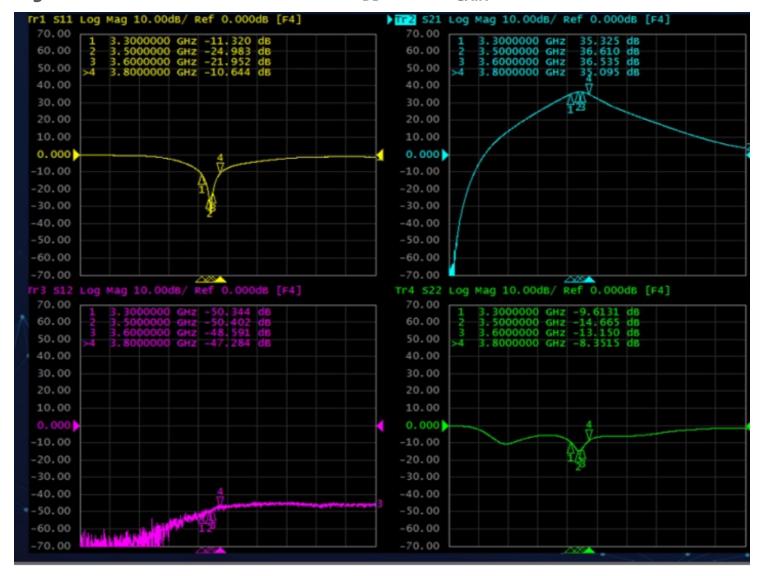
GRF5126 ACLR1 vs Pout at ModulationType = 5G_10M





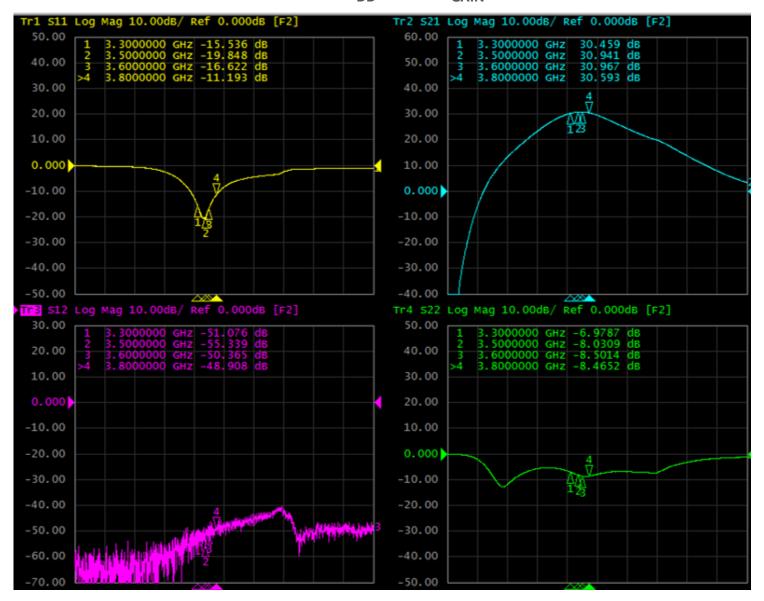
Typical Operating Curves: S-Parameters

High Gain Mode: 3.3 to 3.8 GHz Tune, $V_{DD} = 5 \text{ V}$, $V_{GAIN} = 1.8 \text{ V}$

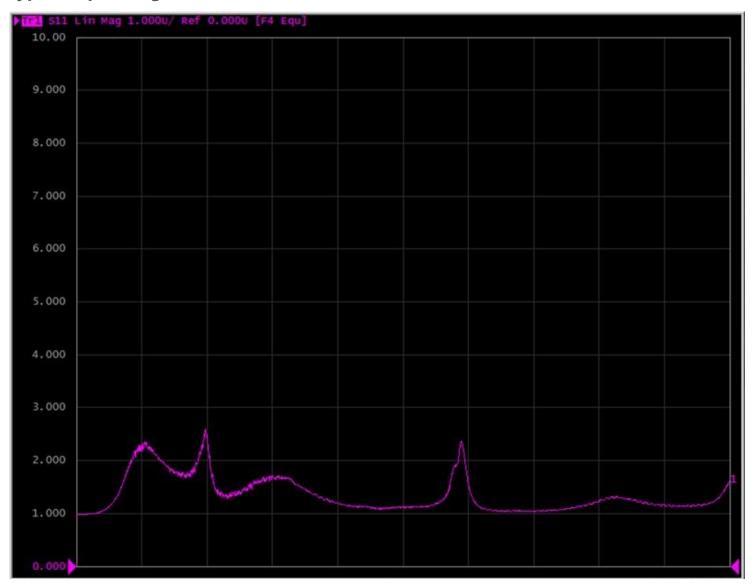


Typical Operating Curves: S-Parameters

Low Gain Mode: 3.3 to 3.8 GHz Tune, $V_{DD} = 5 \text{ V}$, $V_{GAIN} = 0 \text{ V}$

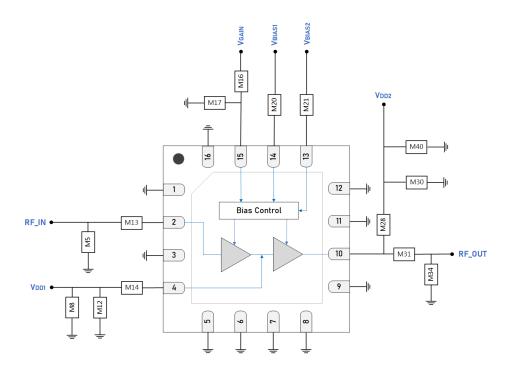


Typical Operating Curves: Mu Factor (10 MHz to 20 GHz)

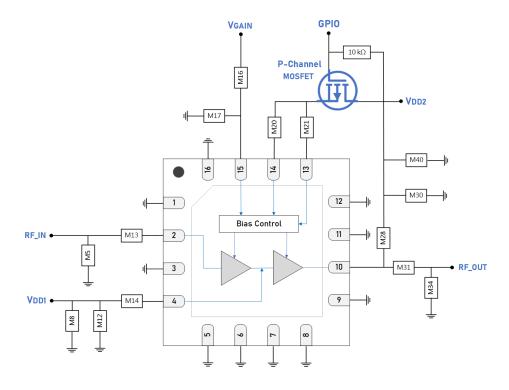


Note: Mu Factor ≥ 1.0 implies unconditional stability.





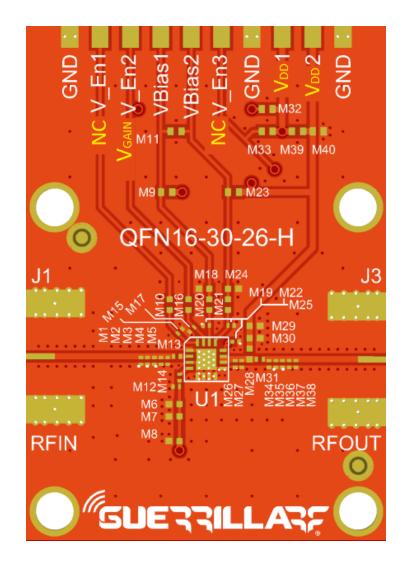
GRF5126 Standard Evaluation Board Schematic



GRF5126 Recommended Schematic for applications using low current GPIO to toggle V_{BIAS1} and V_{BIAS2}



GRF5126 Evaluation Board Assembly Diagram

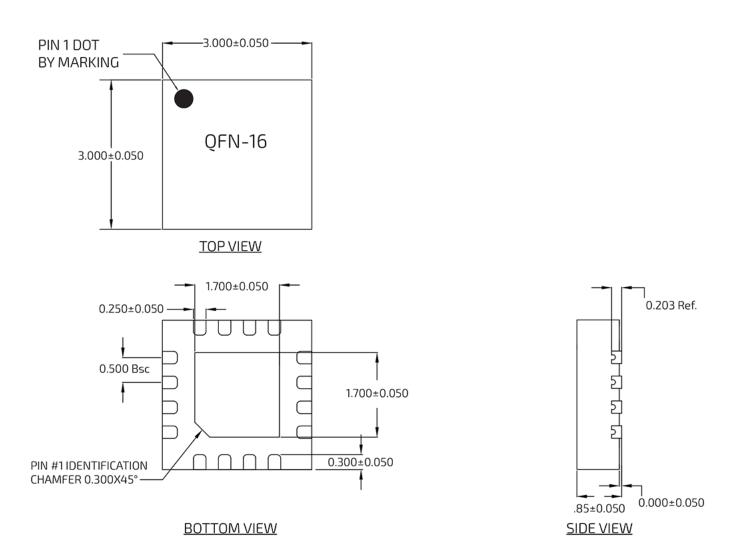




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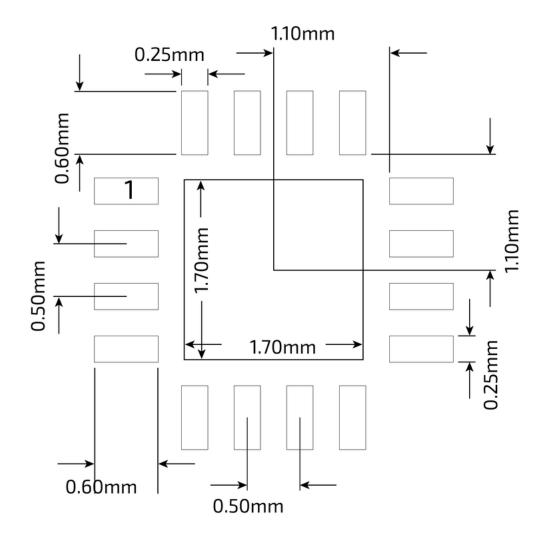
Evaluation Board Assembly Diagram Reference: 3.3 to 3.8 GHz Tune

Component	Туре	Manufacturer	Family	Value	Package Size	Substitution
M5	Inductor	Murata	LQPTN	1.5 nH	0201	ok
M8	Capacitor	Murata	GRM	10 uF	0402	ok
M12	Capacitor	Murata	GRM	0.1 uF	0201	ok
M13	Capacitor	Murata	GJM	3.0 pF	0201	ok
M14	Inductor	Murata	LQPTN	0.7 nH	0201	ok
M16	Resistor (jumper)	Various	5%	0 Ω	0402	ok
M17	Capacitor	Murata	GRM	0.1 uF	0201	ok
M20	Resistor	Various	5%	3.24 kΩ	0402	ok
M21	Resistor	Various	5%	2.7 kΩ	0402	ok
M26	Capacitor	Murata	GRM	0.3 pF	0201	ok
M28	Inductor	Murata	LQW	7.5 nH	0402	ok
M30	Capacitor	Murata	GRM	0.1 uF	0402	ok
M31	Capacitor	Murata	GJM	3.0 pF	0201	ok
M34	Capacitor	Murata	GJM	0.8 pF	0201	ok
M39	Resistor (jumper)	Various	5%	0 Ω	0402	ok
M40	Capacitor	Murata	GRM	10 uF	0402	ok
Evaluation Board	QFN16-30-26-H					



QFN 16 3x3mm Package Dimensions





QFN 16 3x3mm Suggested PCB Footprint (Top View)



Package Marking Diagram



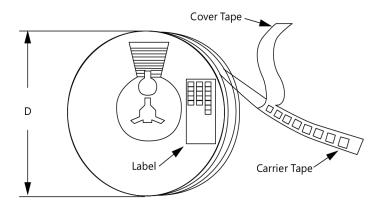
Line 1: "YY" = Year. "WW" = WORK WEEK the Device was assembled.

Line 2: "GRF" = Guerrilla RF

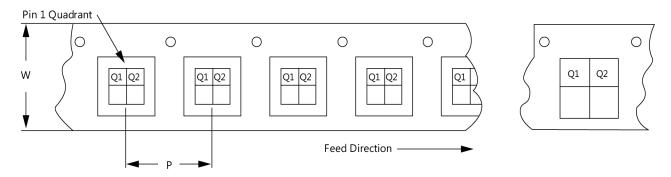
Line 3: "XXXX" = Device Part Number.

Tape and Reel Information

Guerrilla RF's tape and reel specification complies with Electronics Industries Association (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag, and the outside surface of the box. For the latest reel specifications and package information (including units/reel), please visit Package Manufacturing Information | Guerrilla RF (guerrilla-rf.com).



Tape and Reel Packaging with Reel Diameter Noted (D)



Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information



RELEASE Ø DATA SHEET

Revision History

Revision Date	Description of Change
December 21, 2023	Advance Data Sheet.
April 9, 2024	Preliminary Data Sheet.
June 4, 2025	Release Ø Data Sheet.



RELEASE Ø DATA SHEET

Data Sheet Classifications

Data Sheet Status	Notes
Advance	S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices.
Preliminary	All data based on evaluation board measurements taken within the Guerrilla RF Applications Lab. Any MIN/MAX limits represented within the data sheet are based solely on <i>estimated</i> part-to-part variations and process spreads. All parametric values are subject to change pending the collection of additional data.
Release Ø	All data based on measurements taken with <i>production-released</i> material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using <i>modelled estimates</i> that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory.
Release A-Z	All data based on measurements taken with production-released material derived from multiple lots which have been fabricated over an extended period of time. MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads.

Information in this data sheet is specific to the Guerrilla RF, Inc. ("Guerrilla RF") product identified.

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