

GRF5225

HIGH EFFICIENCY POWER AMPLIFIER 2.3 to 2.7 GHz

FEATURES

- Utilizing DPD:
 - +22 dBm Linear Output Power
 - PAE = 29 %
 - ACLR \leq -52 dBc
 - LTE 10 MHz Downlink CFR 8.2 dB
- 39 mA Native Mode Quiescent Current Consumption
- 4 V Nominal Supply Voltage
- 50 Ω Single-ended Input and Output Impedances
- Digital Shutdown
- Rugged Design is Extremely Resilient to Mismatched Loads
- 40 to 85 °C Operating Temperature Range
- Compact 3 x 3 mm QFN-16 Package

Reference: 4 V / 39 mA I_{CCQ} / 2.5 GHz

- Gain: 27.8 dB (22 dBm Pout)
- PAE: 29 % (22 dBm Pout)
- Evaluation Board Noise Figure: TBD

APPLICATIONS

- Cellular Boosters
- Automotive Compensators
- Picocells/Femtocells
- Customer Premise Equipment

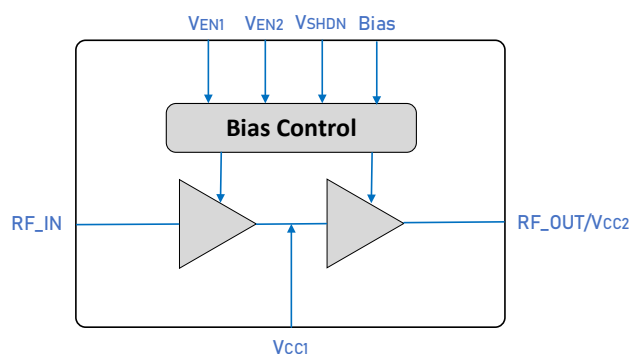
DESCRIPTION

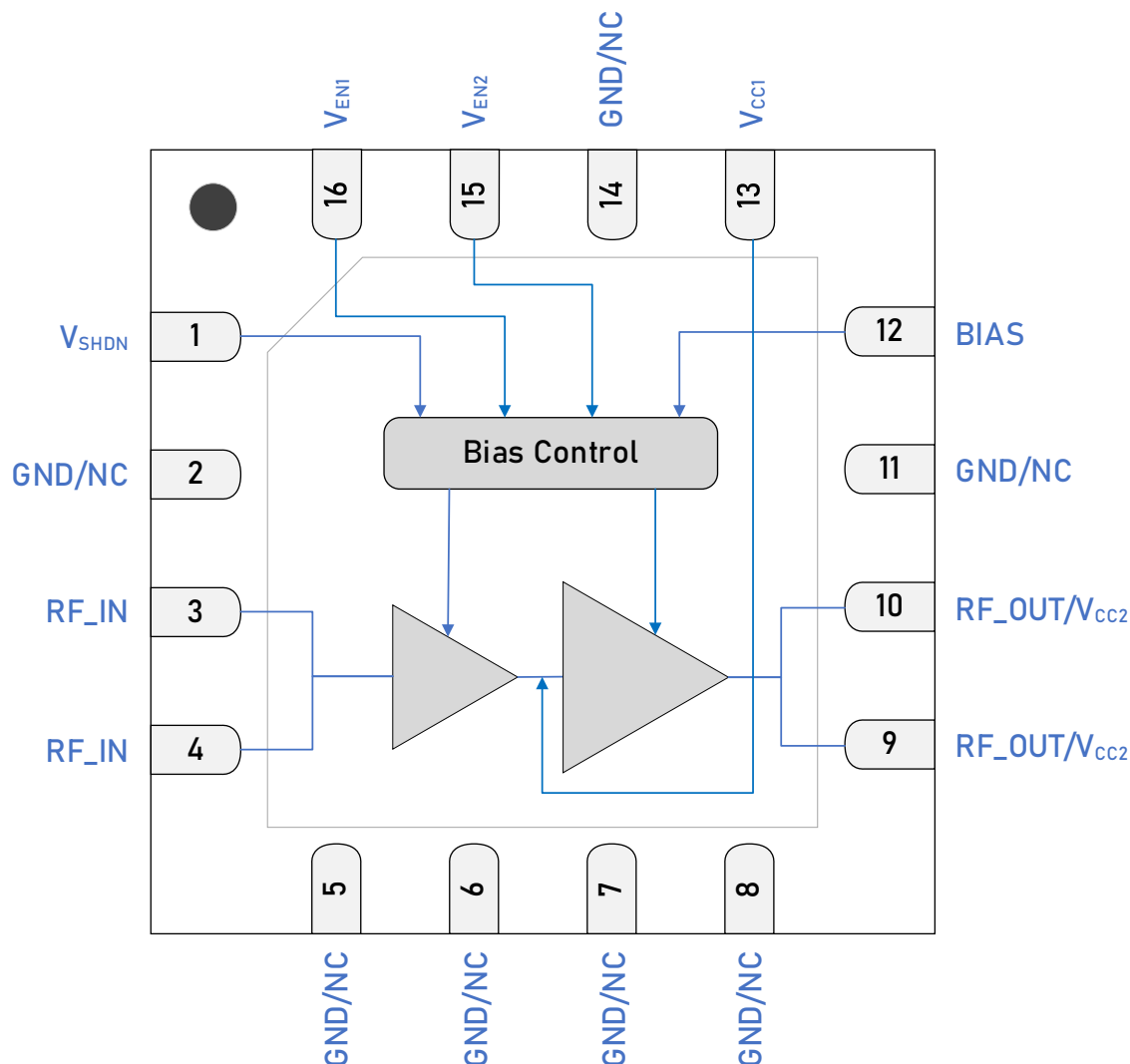
The GRF5225 is a high gain, two-stage InGaP HBT power amplifier designed to deliver excellent ACLR performance over the 2.3 to 2.7 GHz band using DPD (digital predistortion).

Please consult with the GRF applications engineering team for custom tuning/evaluation board data.

Additional tunes can be found on the GRF5225 "Custom Tunes" product page: [GRF5225 Custom Tunes](#)

BLOCK DIAGRAM





3 x 3 mm QFN-16 Pin Out (Top View)

Pin Assignments

Pin	Name	Description	Note
1	V _{SHDN}	Digital Shutdown Pin	V _{SHDN} ≥ 1.8 V (Logic HIGH) disables device. V _{SHDN} ≤ 0.8 V (Logic LOW) enables device.
2, 5, 6, 7, 8, 11, 14	GND/NC	Ground or No Connect	No internal connection to die. These pins can be left unconnected, or be connected to ground (recommended). Use a via as close to the pin as possible if grounded.
3, 4	RF_IN	RF Input	Pins 3 and 4 tied together on system board. An external DC blocking capacitor must be used.
9, 10	RF_OUT/V _{CC2}	PA Output/Bias Voltage	Pins 9 and 10 tied together on system board. V _{CC2} must be applied to this pin via an RF choke.
12	Bias	Bias Circuit Supply	Connect to V _{CC2} through external resistor.
13	V _{CC1}	Bias Voltage	Connect to V _{CC1} through external inductor with capacitive termination above (see applications schematic).
15	V _{EN2}	Enable2 Voltage Input	V _{EN2} and series resistor set I _{CCQ} for the output stage. V _{EN2} ≤ 0.2 volts disables stage 2.
16	V _{EN1}	Enable1 Voltage Input	V _{EN1} and series resistor set I _{CCQ} for the input stage. V _{EN1} ≤ 0.2 volts disables stage 1.
PKG BASE	GND	Ground	Provides DC and RF ground for the amplifier, as well as thermal heat sink. Recommend multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page.

Truth Table

Pin	Logic	Condition
V _{SHDN}	LOW	Full Operation
	HIGH	All Amplifiers Off
V _{EN1}	LOW	Stage 1 Amplifier Off
	HIGH	Stage 1 Amplifier On
V _{EN2}	LOW	Stage 2 Amplifier Off
	HIGH	Stage 2 Amplifier On

Absolute Ratings

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage		V_{CC}	0	5.25	V
RF Input Power	50 Ω , $V_{CC} = 5$ V, CW Tone, 100% Duty Cycle, $T_{PKG\ BASE} = 25^{\circ}\text{C}$.	$P_{IN\ MAX - 1:1}$		TBD	dBm
	Load VSWR $\leq 8:1$, all phase angles, $V_{CC} = 5$ V, CW Tone, 100% Duty Cycle, $T_{PKG\ BASE} = -40$ to 85°C .	$P_{IN\ MAX - 8:1}$		TBD	
Operating Temperature (Package Base).		$T_{PKG\ BASE}$	-40	85	$^{\circ}\text{C}$
Maximum Junction Temperature (MTTF $> 10^6$ Hours).		$T_{J\ MAX}$		TBD	$^{\circ}\text{C}$
Maximum Dissipated Power: Stage 1: DC only (no RF applied).		$P_{DISS\ MAX}$		* 200	mW
Maximum Dissipated Power: Stage 2: DC only (no RF applied).		$P_{DISS\ MAX}$		* 500	mW
Shutdown Voltage		V_{SHDN}		** 5.25	V

Electrostatic Discharge

Human Body Model	HBM	TBD		V
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Storage

Storage Temperature	T_{STG}	-65	150	$^{\circ}\text{C}$
Moisture Sensitivity Level	MSL		1	--

* Bias resistors M5/M9 have been empirically optimized for linearity. Thus, there will be no benefit in decreasing resistance (thereby increasing I_{CCQ}).

** $M4 = 0\ \Omega$. $V_{SHDN} = 4$ V yields $I_{SHDN} = 540\ \mu\text{A}$. I_{SHDN} decreases linearly vs V_{SHDN} (to $65\ \mu\text{A}$ with $V_{SHDN} = 1.8$ V).

Said linear relationship can be used to scale M4 for higher V_{SHDN} voltage: use the pin condition $V_{SHDN_pin}/I_{SHDN} = 2.4\text{V}/147\ \mu\text{A}$.

Calculate M4 for $V_{SHDN}/I_{SHDN} = 4\text{V}/147\ \mu\text{A}$: $M4 = (4-2.4)/(0.000147) = 10.9\ \text{k}\Omega$.



Caution! ESD Sensitive Device.

Exceeding Absolute Maximum Rating conditions may cause permanent damage.

Note: For additional information, please refer to [Manufacturing Note MN-001 — Package and Manufacturing Information](#).



All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging requiring no exemptions. Additional information for this topic can be found at this link - [Environmental and Restricted Substance Statement Library](#)

Recommended Operating Conditions

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	3	4	5.25	V	
Operating Temperature (package base)	$T_{PKG\ BASE}$	-40		85	°C	
RF Frequency Range	F_{RF}	2.3	2.5	2.7	GHz	Typical application schematic using the 2.3 to 2.7 GHz tuning set (notes 1 & 2).
RF_IN Port Impedance	Z_{RFIN}		50		Ω	Single-ended with 1-element match.
RF_OUT Port Impedance	Z_{RFOUT}		50		Ω	Single-ended with 5-element match.

Note 1: Operation outside of this range is supported by using different custom tunes. Examples of other optimized tunes can be found here: [GRF5225 Custom Tunes](#).

Note 2: Contact the Guerrilla RF Applications team for guidance on optimizing the tuning of the device for alternative bands.

Nominal Operating Parameters – General

The following conditions apply unless noted otherwise: typical application schematic using the 2.3 to 2.7 GHz tuning set. $V_{CC} = 4\text{ V}$, $V_{SHDN} = \text{LOW}$, $I_{CCQ} = 39\text{ mA}$, $M5 = 3.0\text{ k}\Omega$, $M9 = 3.83\text{ k}\Omega$, $P_{OUT} = 22\text{ dBm}$, $F_{TEST} = 2.5\text{ GHz}$, $50\text{ }\Omega$ system impedance, $T_{PKG\text{ BASE}} = 25\text{ }^{\circ}\text{C}$. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Supply Quiescent Current	I_{CCQ}		39		mA	$I_{CCQ1} + I_{CCQ2}$, no RF applied.
Supply Current with RF Applied	I_{CC}		150		mA	$I_{CC1} + I_{CC2}$, $P_{OUT} = 22\text{ dBm}$.
Enable Current 1	$I_{ENABLE1}$		1		mA	$V_{CC}/V_{EN1}/V_{EN2} = 4\text{ V}$.
Enable Current 2	$I_{ENABLE2}$		0.5		mA	$V_{CC}/V_{EN1}/V_{EN2} = 4\text{ V}$.
Operating Temperature Range	$T_{PKG\text{ BASE}}$	-40		85	$^{\circ}\text{C}$	Measured on Package Base.
Logic Input Low	V_{IL}	0		0.8	V	Applies to V_{SHDN} Input.
Logic Input High	V_{IH}	1.8		V_{CC}	V	Applies to V_{SHDN} Input.
Logic Current Low	I_{IL}		1.3		nA	Applies to V_{SHDN} Input, $V_{IL} = 0.8\text{ V}$.
Logic Current High	I_{IH}		65		μA	Applies to V_{SHDN} Input, $V_{IH} = 1.8\text{ V}$.
			265			Applies to V_{SHDN} Input, $V_{IH} = 3.3\text{ V}$.
Switching Rise Time	T_{RISE}		TBD		ns	Applies to V_{SHDN} Input.
Switching Fall Time	T_{FALL}		TBD		ns	Applies to V_{SHDN} Input.

Disabled Mode

Supply Quiescent Current	$I_{CCQ\text{-SHDN}}$		7.5		μA	$V_{CC} = 4\text{ V}$, $V_{SHDN}/V_{EN1}/V_{EN2} = \text{HIGH}$.
Enable Current 1	$I_{ENABLE1\text{-SHDN}}$		1.1		mA	$V_{CC} = 4\text{ V}$, $V_{SHDN}/V_{EN1}/V_{EN2} = \text{HIGH}$.
Enable Current 2	$I_{ENABLE2\text{-SHDN}}$		1.1		mA	$V_{CC} = 4\text{ V}$, $V_{SHDN}/V_{EN1}/V_{EN2} = \text{HIGH}$.

Thermal Data (Stage 1 and Stage 2)

See plot of Junction Temp vs. Output Power			TBD			On standard evaluation board.
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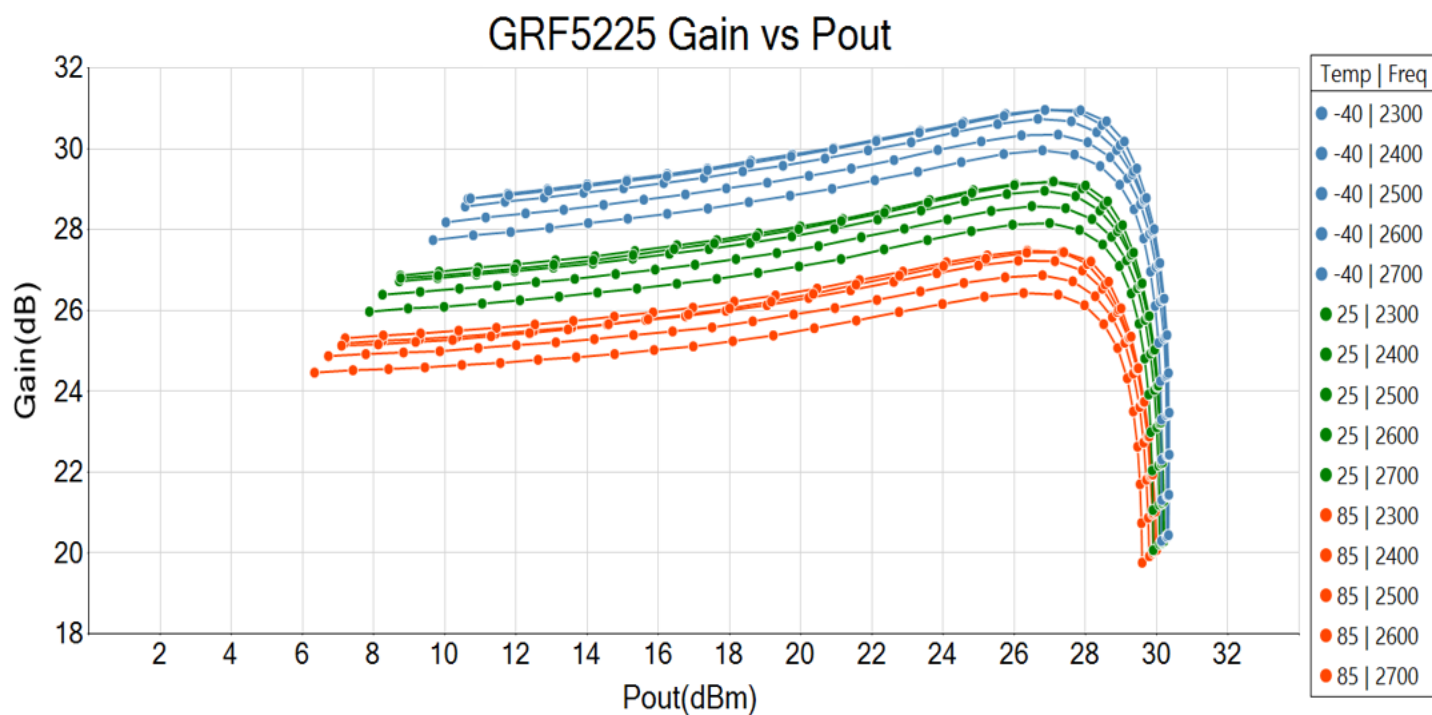
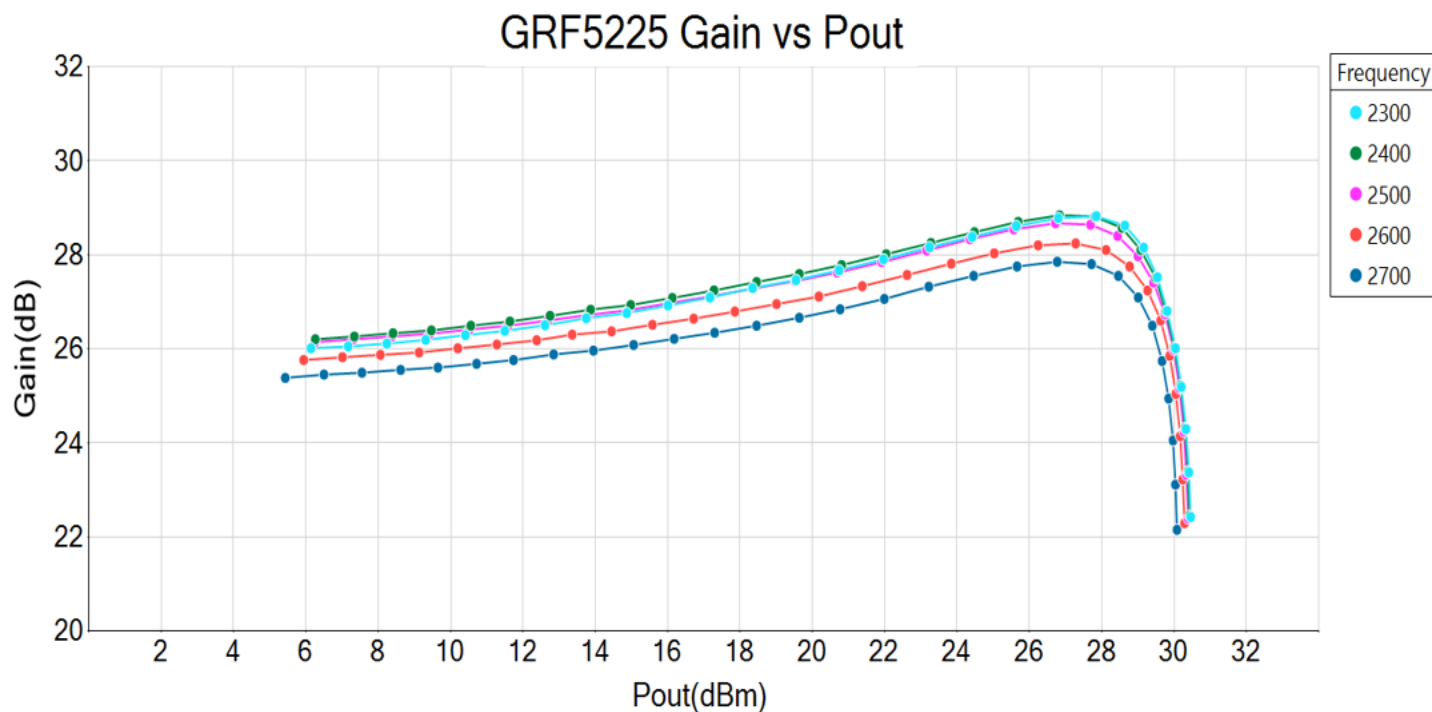
Nominal Operating Parameters – RF: 2.3 to 2.7 GHz, 4 V Operation

The following conditions apply unless noted otherwise: Typical Application Schematic using the 2.3 to 2.7 GHz tuning set. $V_{CC} = 4\text{ V}$, $V_{SHDN} = \text{LOW}$, $I_{CCQ} = 39\text{ mA}$, $M5 = 3.0\text{ k}\Omega$, $M9 = 3.83\text{ k}\Omega$, $P_{OUT} = 22\text{ dBm}$, $F_{TEST} = 2.5\text{ GHz}$, $50\text{ }\Omega$ system impedance, $T_{PKG\text{ BASE}} = 25\text{ }^{\circ}\text{C}$. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Small Signal Gain	S21		26.5		dB	$V_{CC} = 4\text{ V}$, $F_{TEST} = 2.5\text{ GHz}$, $P_{IN} = -9\text{ dBm}$.
Standby Mode Gain	S21 _{STBY}		-35		dB	Disabled Mode: $V_{SHDN}/V_{EN1}/V_{EN2} = \text{HIGH}$. $P_{IN} = 0\text{ dBm}$.
Input Return Loss	S11		< -10		dB	$F_{RF} = 2.3\text{ to }2.7\text{ GHz}$.
Output Return Loss	S22		< -3.5		dB	$F_{RF} = 2.3\text{ to }2.7\text{ GHz}$.
Reverse Isolation	S12		< -40		dB	$F_{RF} = 2.3\text{ to }2.7\text{ GHz}$.
Noise Figure	NF		TBD		dB	On standard evaluation board.
Saturated Output Power	Psat		30.4		dBm	$V_{CC} = 4\text{ V}$, $F_{TEST} = 2.5\text{ GHz}$ (sine wave input).
Adjacent Channel Leakage Ratio	ACLR		-52		dBc	$V_{CC} = 4\text{ V}$, $P_{OUT} = 22\text{ dBm}$, LTE 10 MHz Downlink CFR 8.2 dB, $F_{TEST} = 2.3\text{ to }2.7\text{ GHz}$ (note 3).

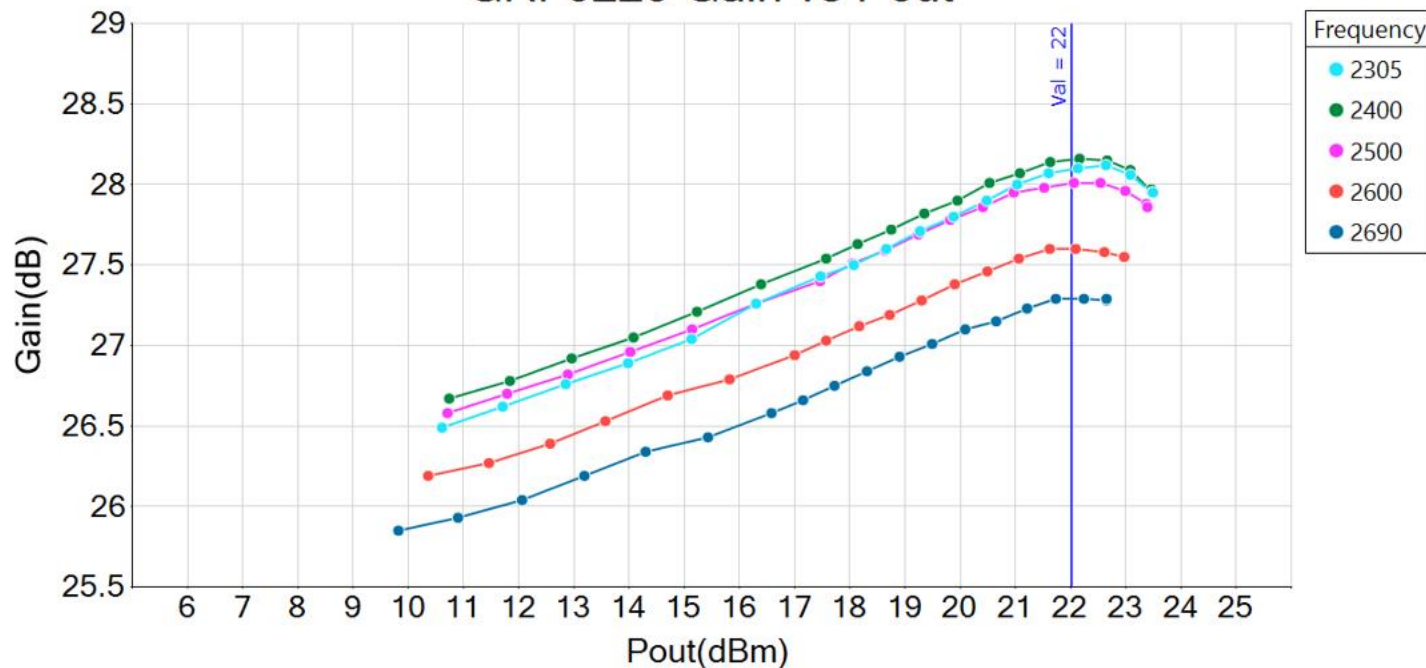
Note 3: MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. As additional production lots are fabricated, accumulated test data will be used to refine the MIN/MAX limits.

GRF5225 Typical Operating Curves: 2.3 to 2.7 GHz Tune (CW)

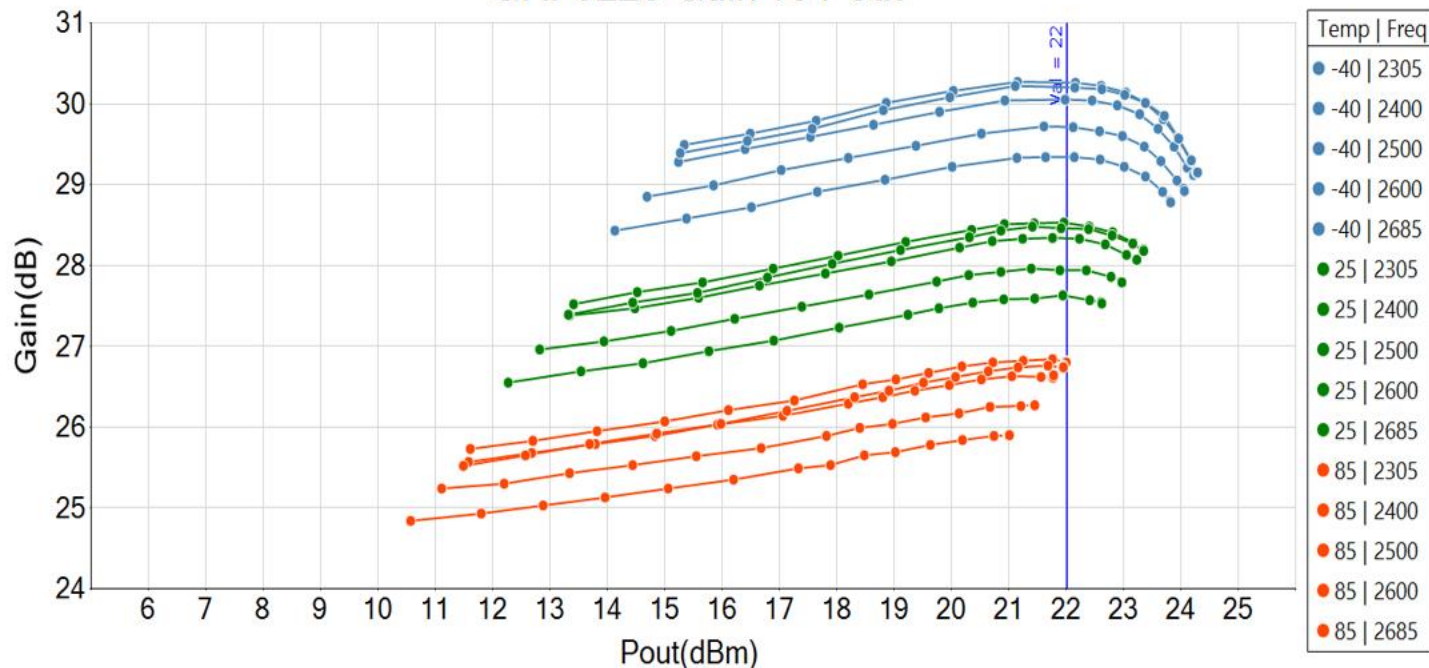


GRF5225 Typical Operating Curves: 2.3 to 2.7 GHz Tune (Modulated with DPD)

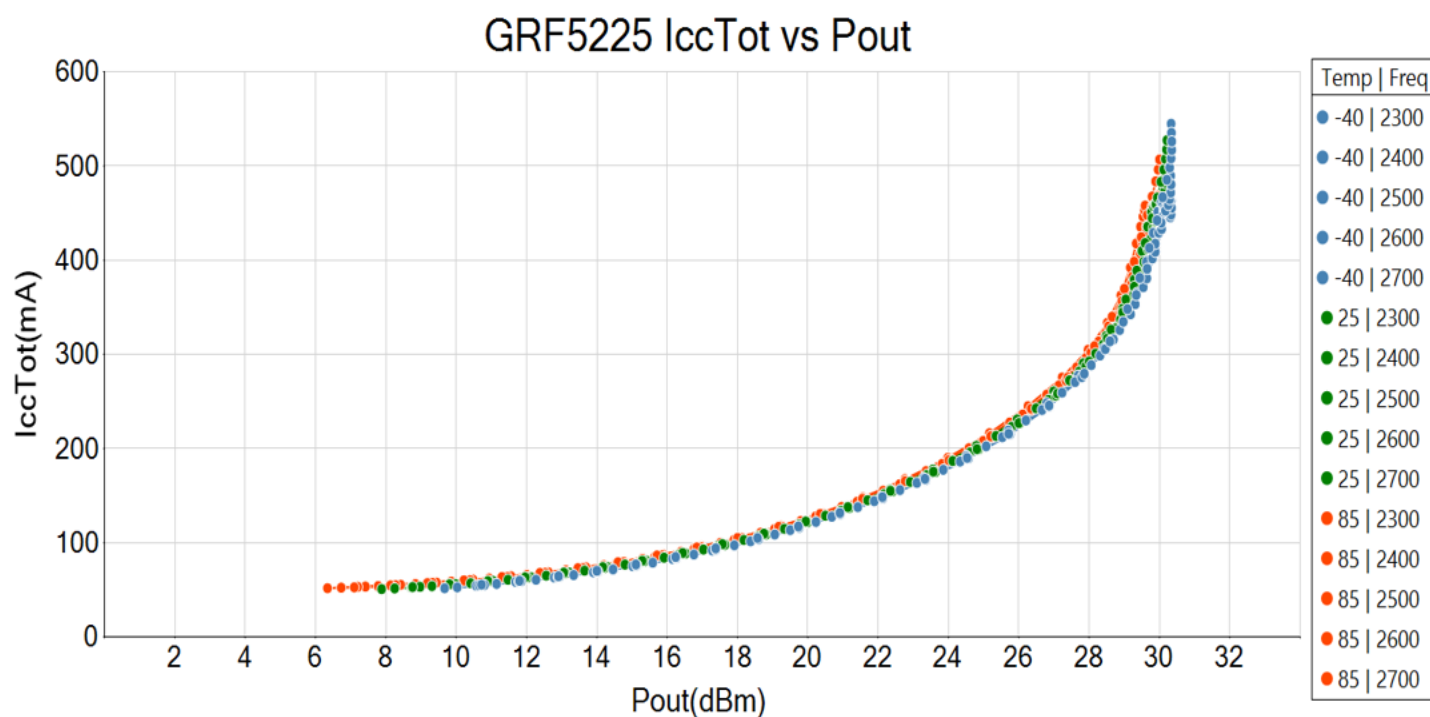
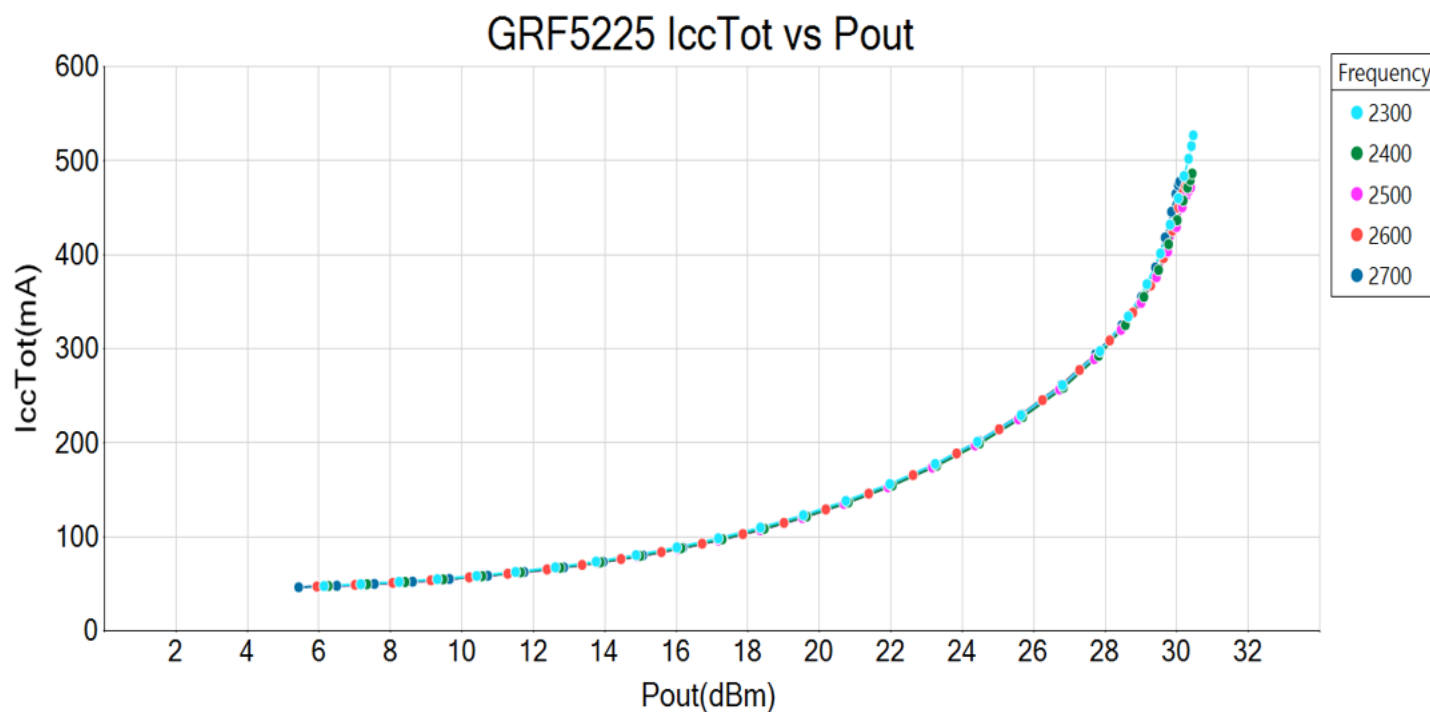
GRF5225 Gain vs Pout



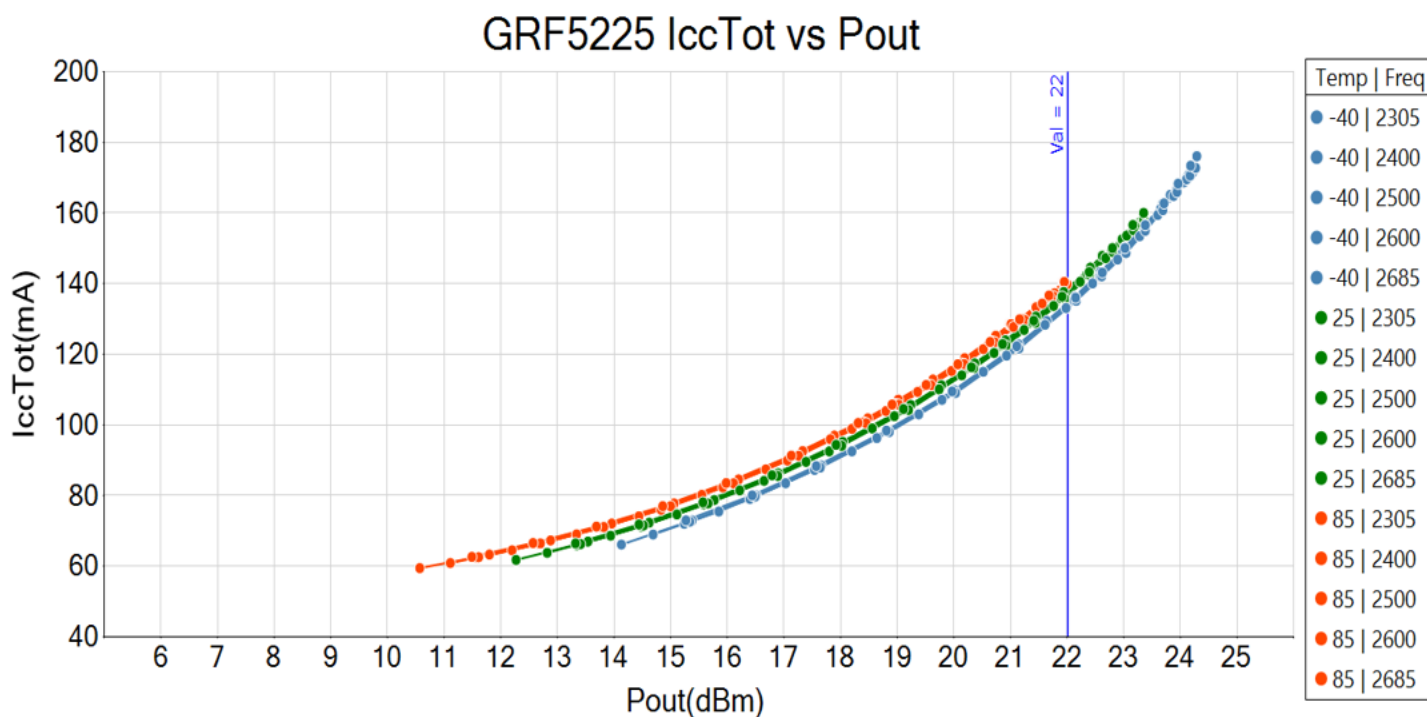
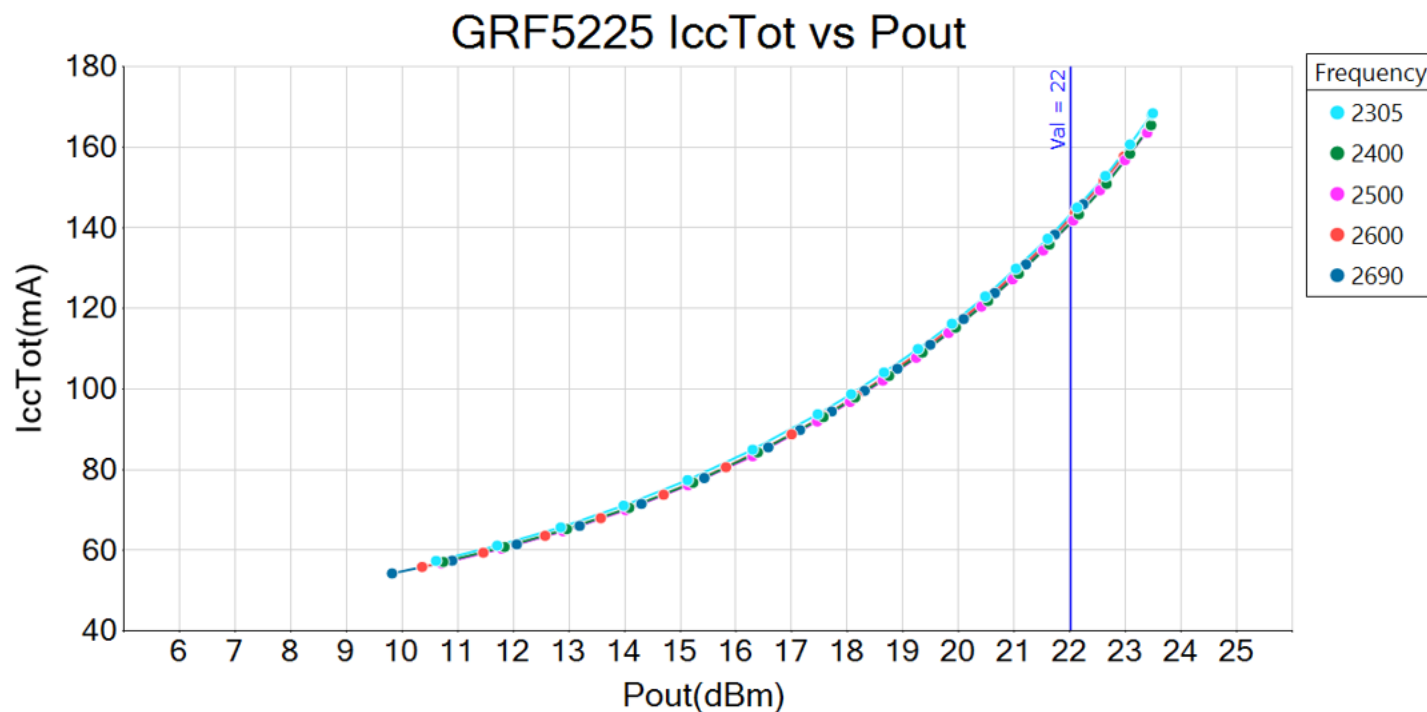
GRF5225 Gain vs Pout



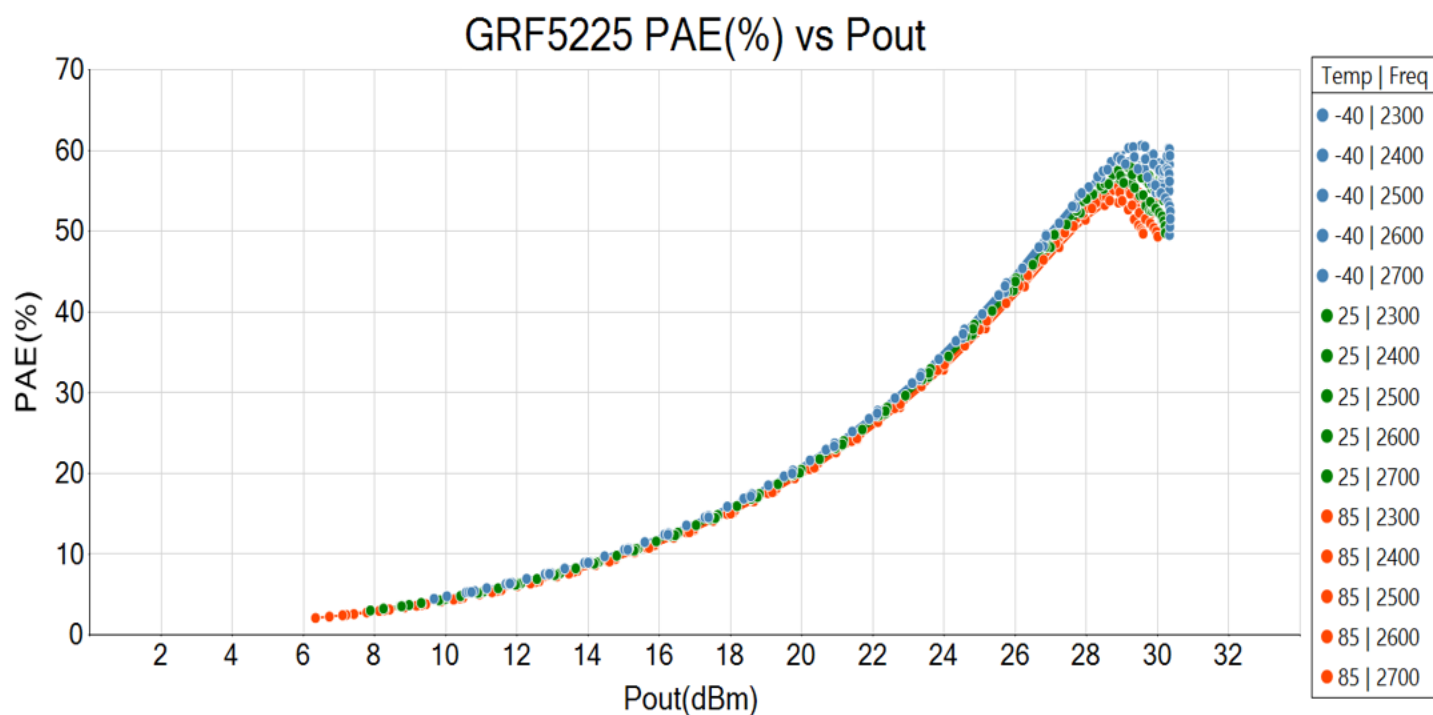
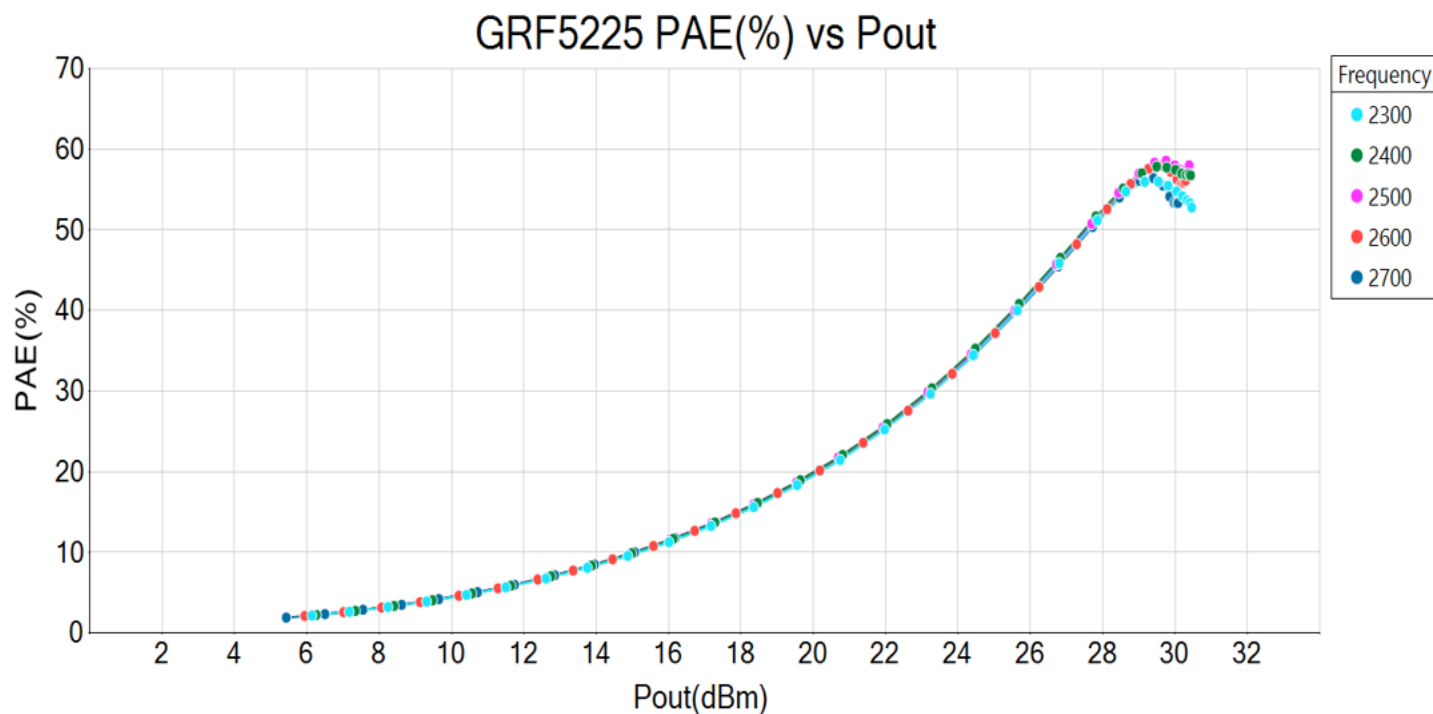
GRF5225 Typical Operating Curves: 2.3 to 2.7 GHz Tune (CW)



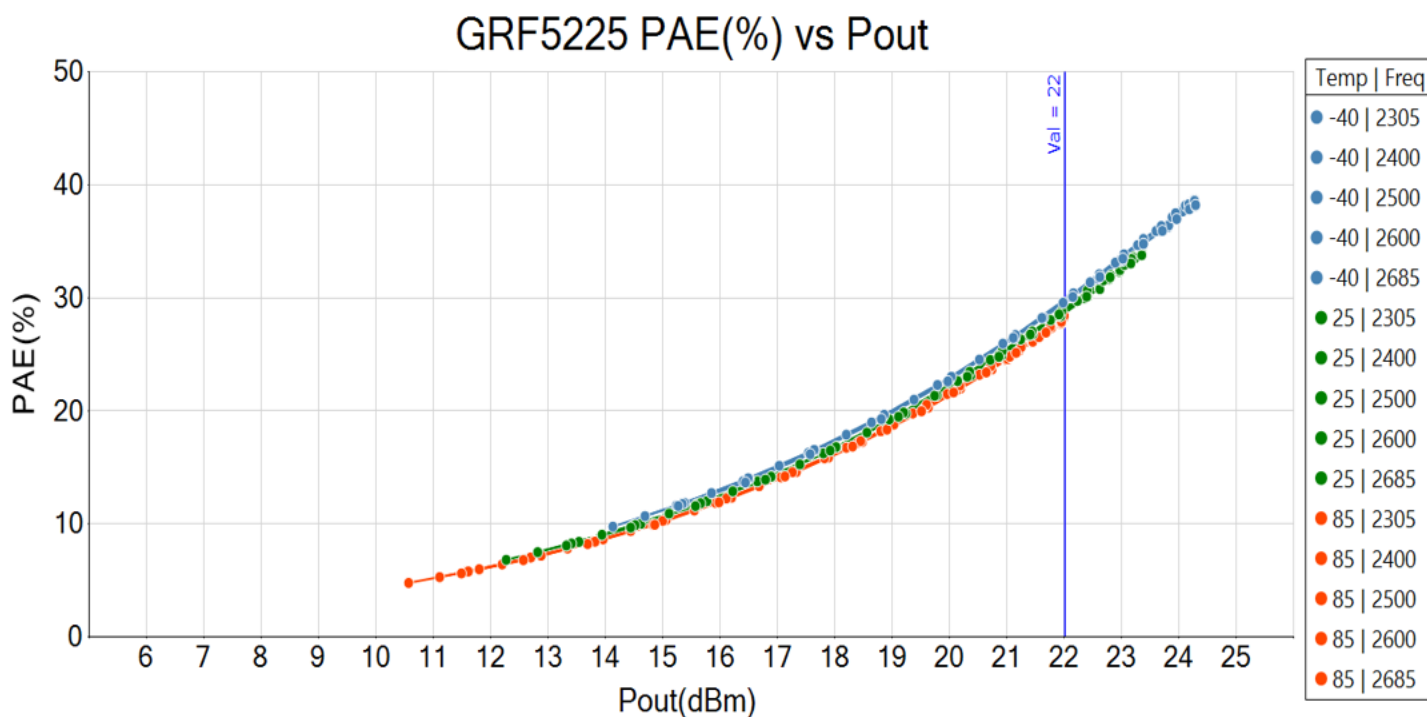
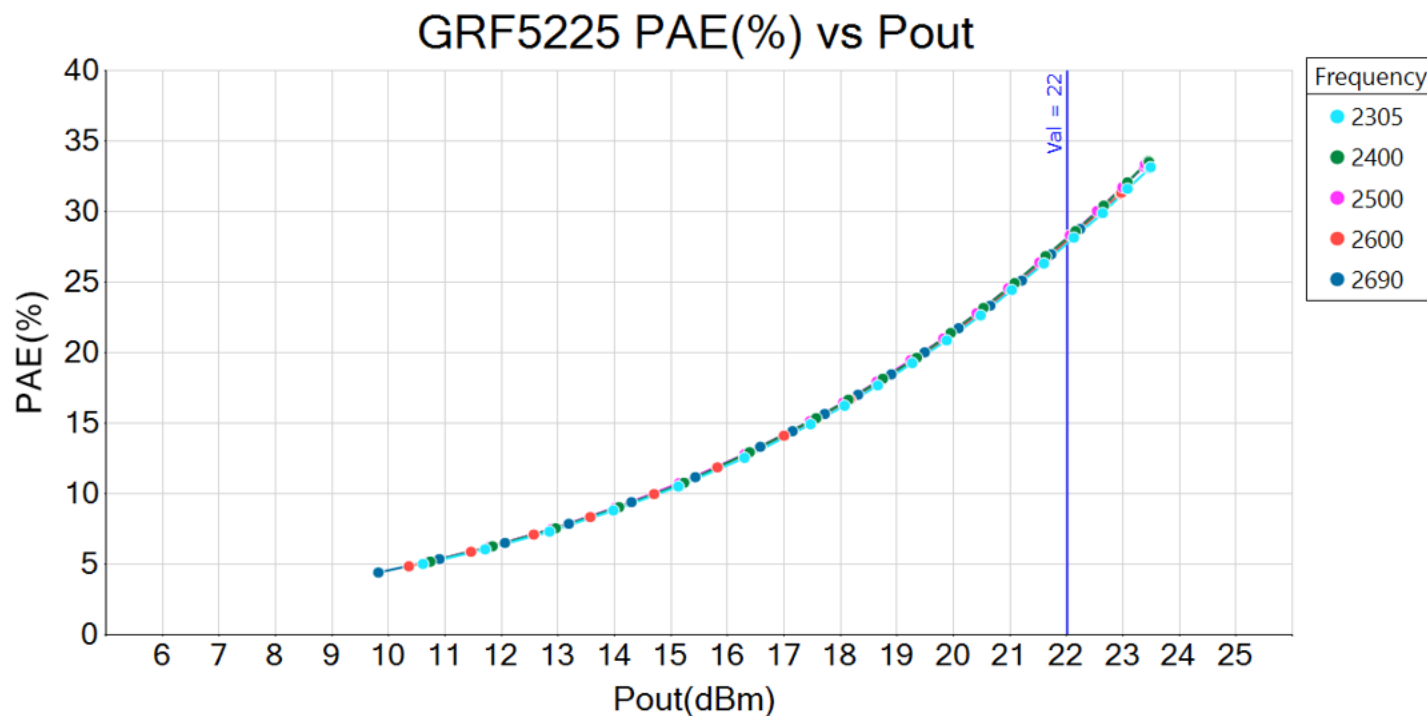
GRF5225 Typical Operating Curves: 2.3 to 2.7 GHz Tune (Modulated with DPD)



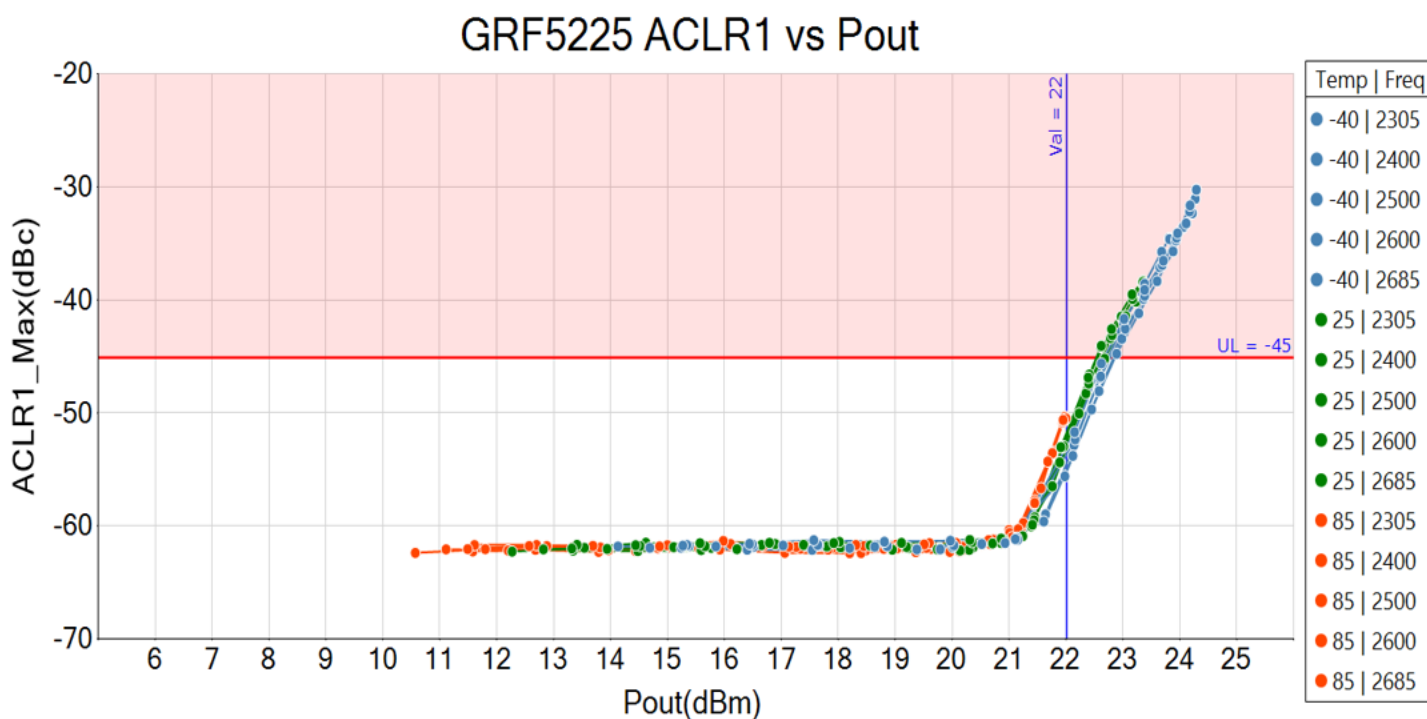
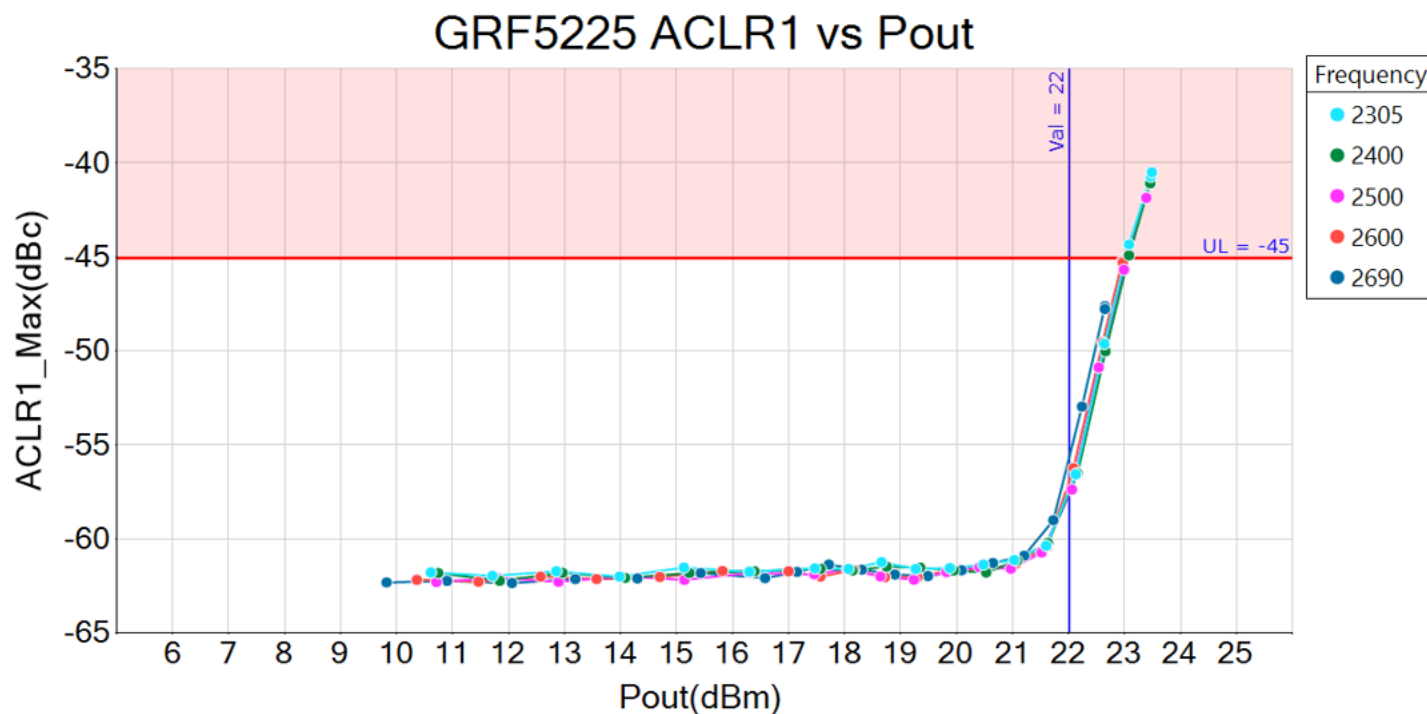
GRF5225 Typical Operating Curves: 2.3 to 2.7 GHz Tune (CW)



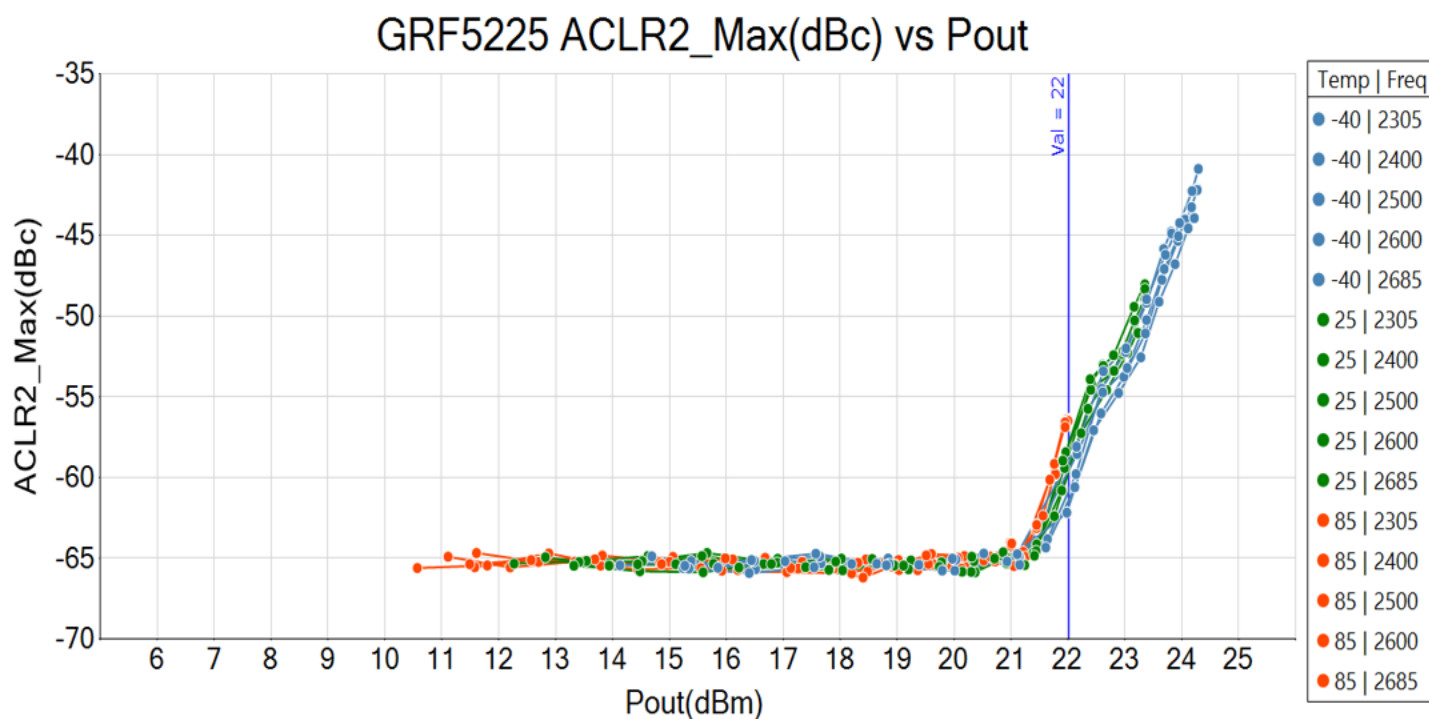
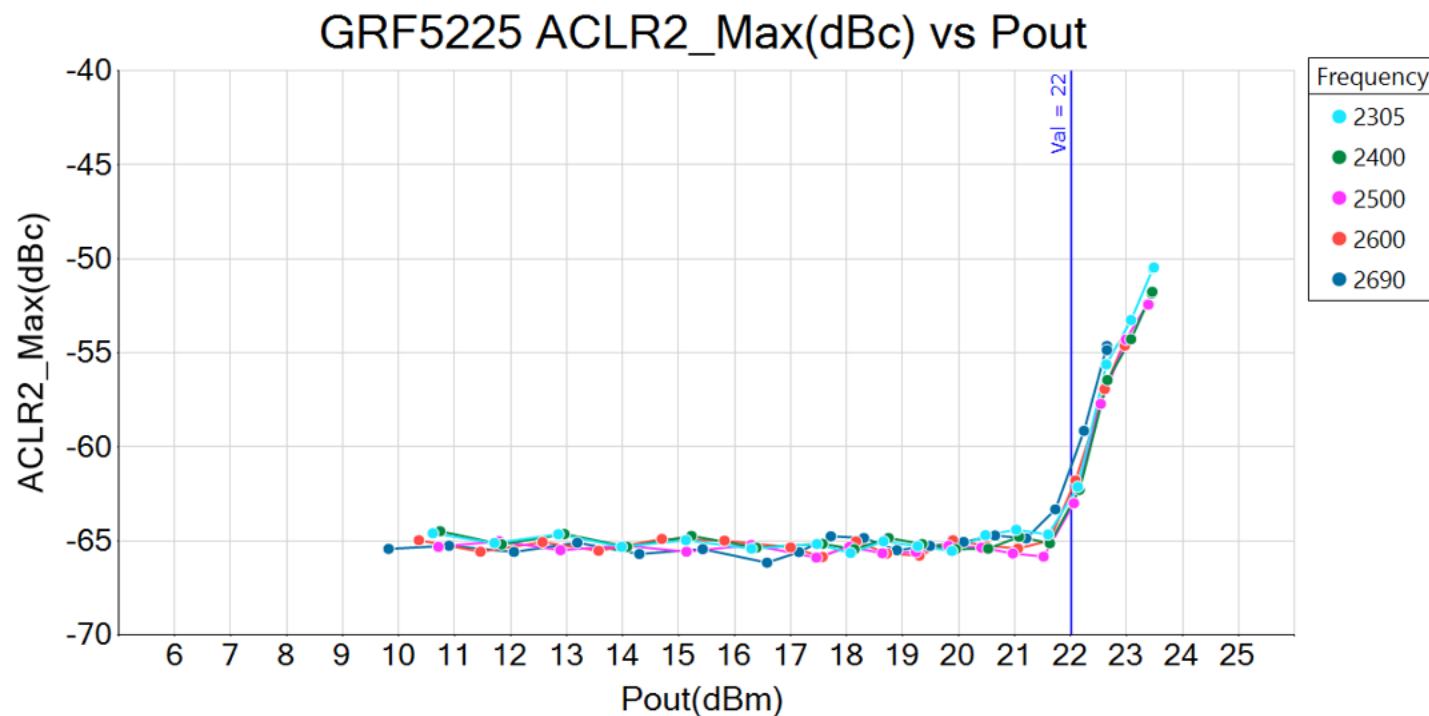
GRF5225 Typical Operating Curves: 2.3 to 2.7 GHz Tune (Modulated with DPD)

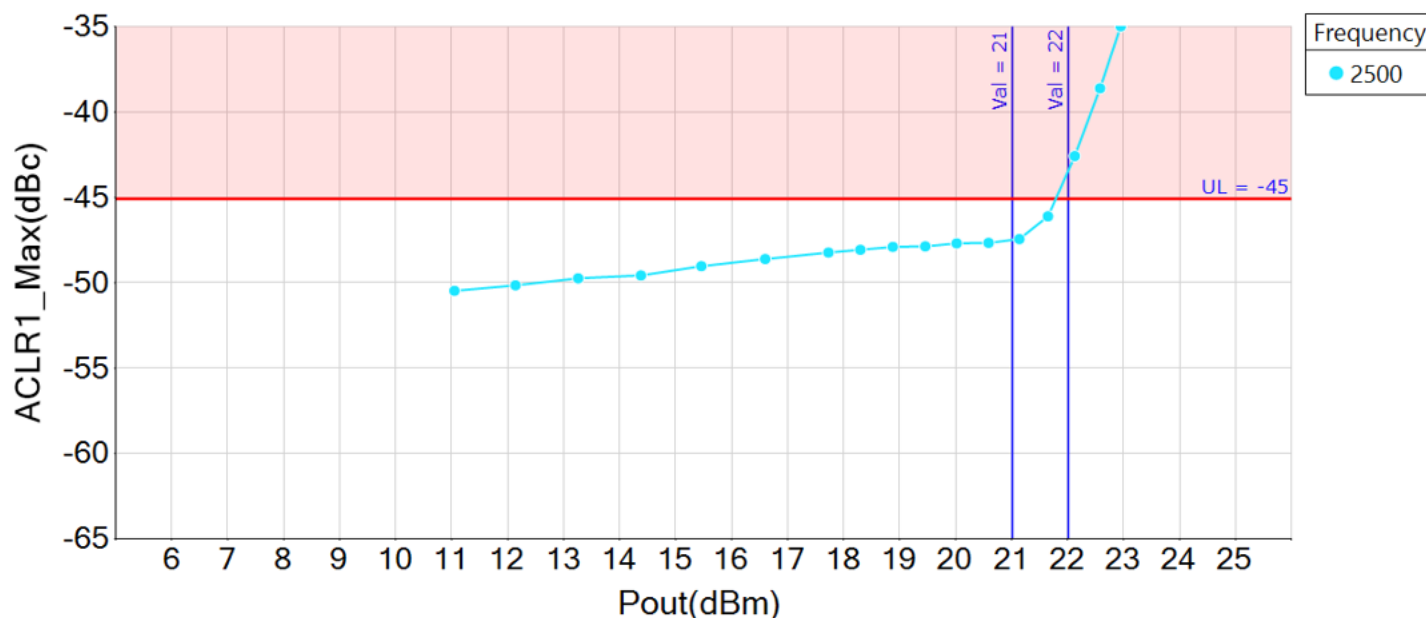
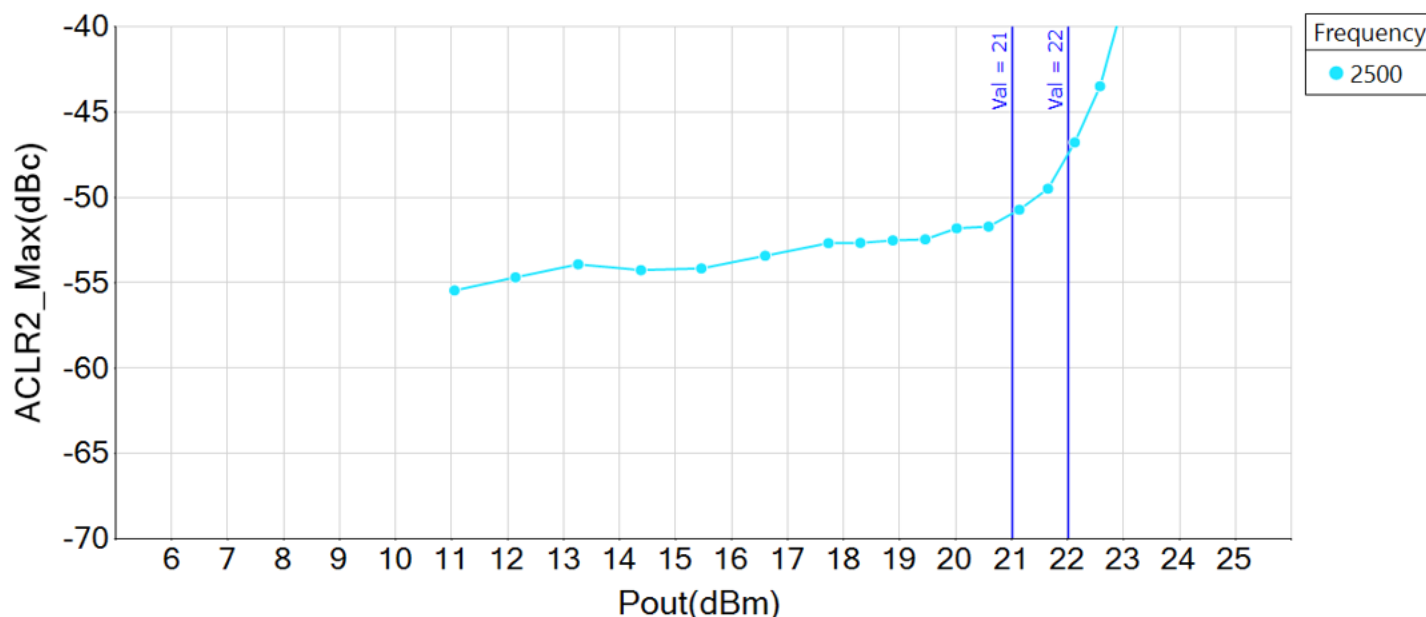


GRF5225 Typical Operating Curves: 2.3 to 2.7 GHz Tune (Modulated with DPD)

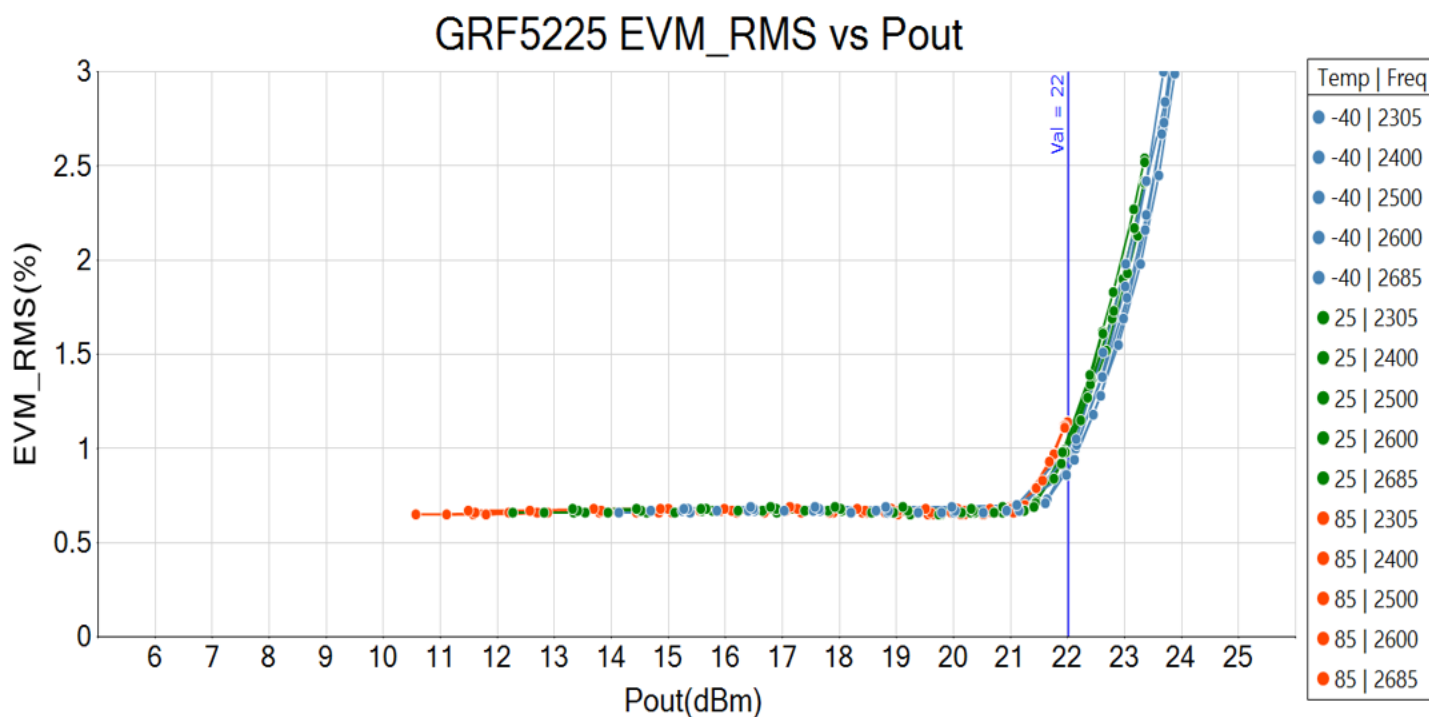
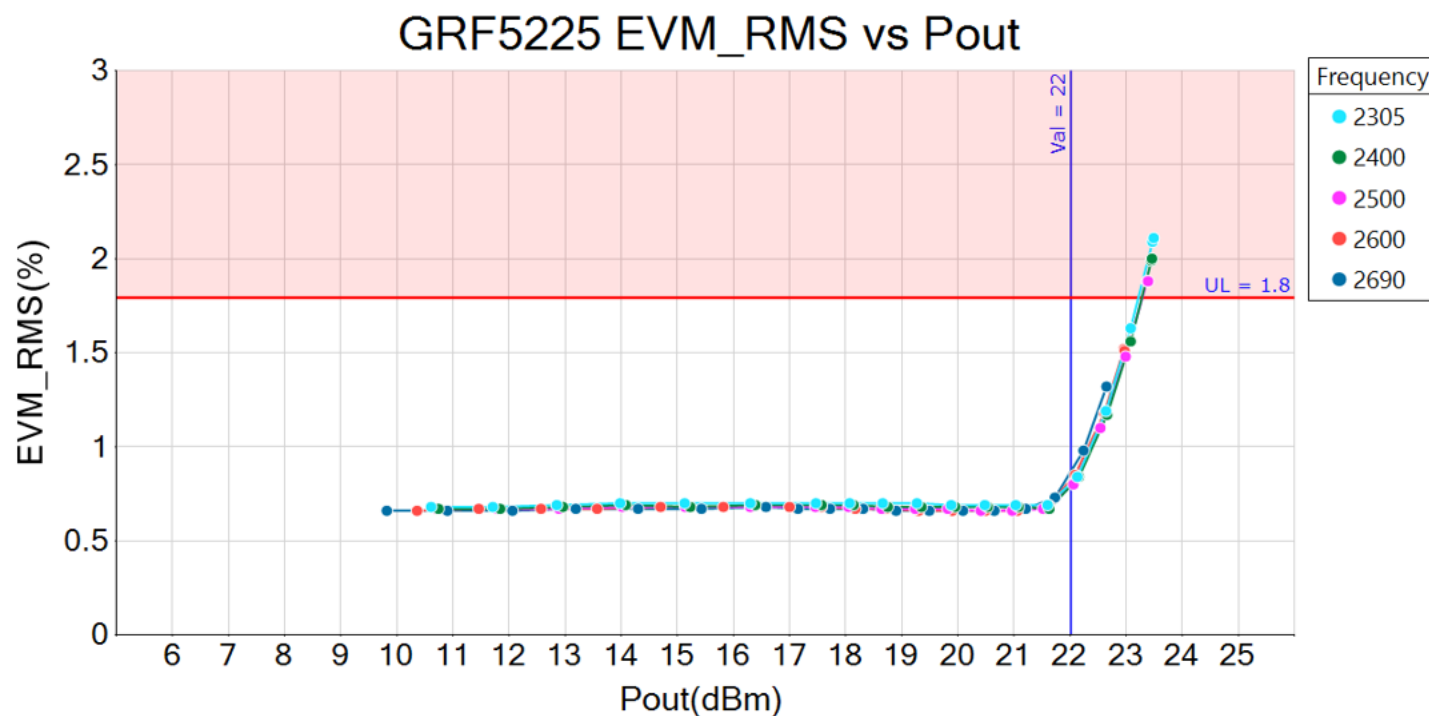


GRF5225 Typical Operating Curves: 2.3 to 2.7 GHz Tune (Modulated with DPD)

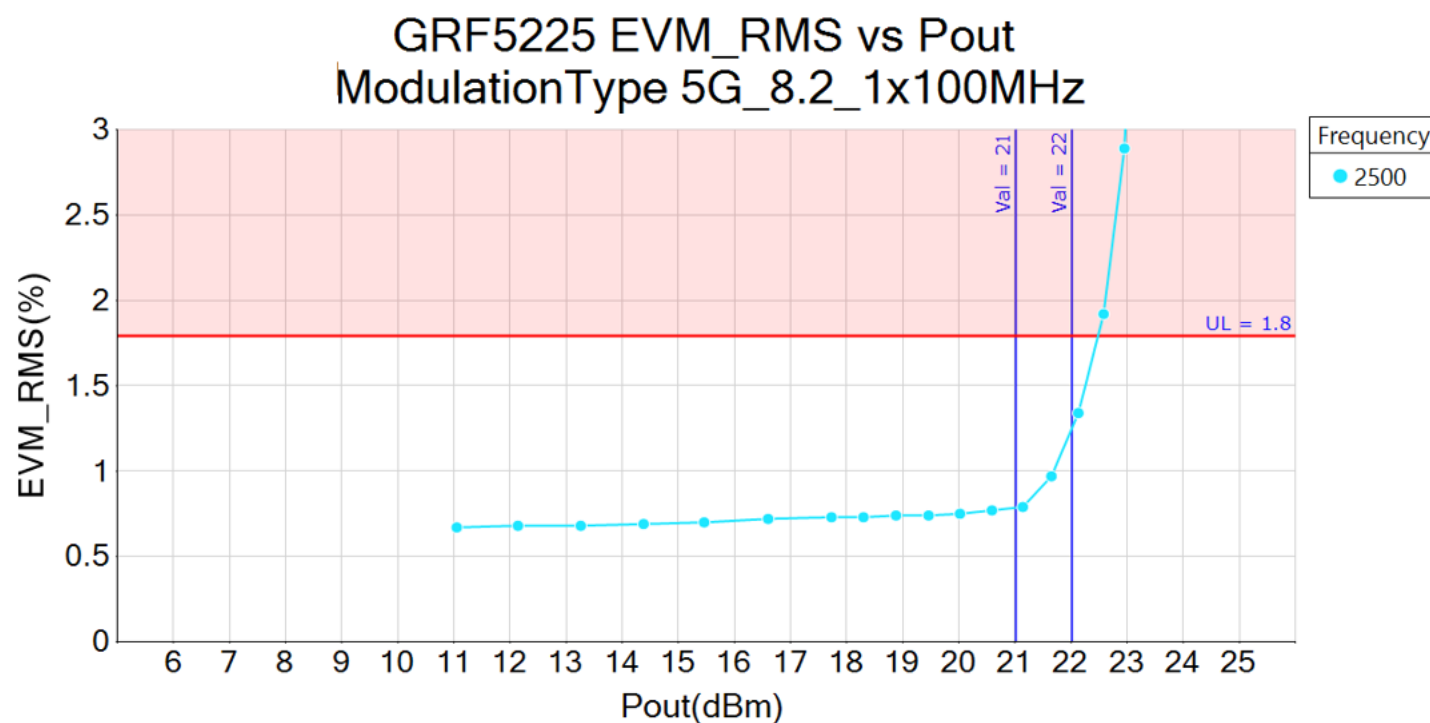


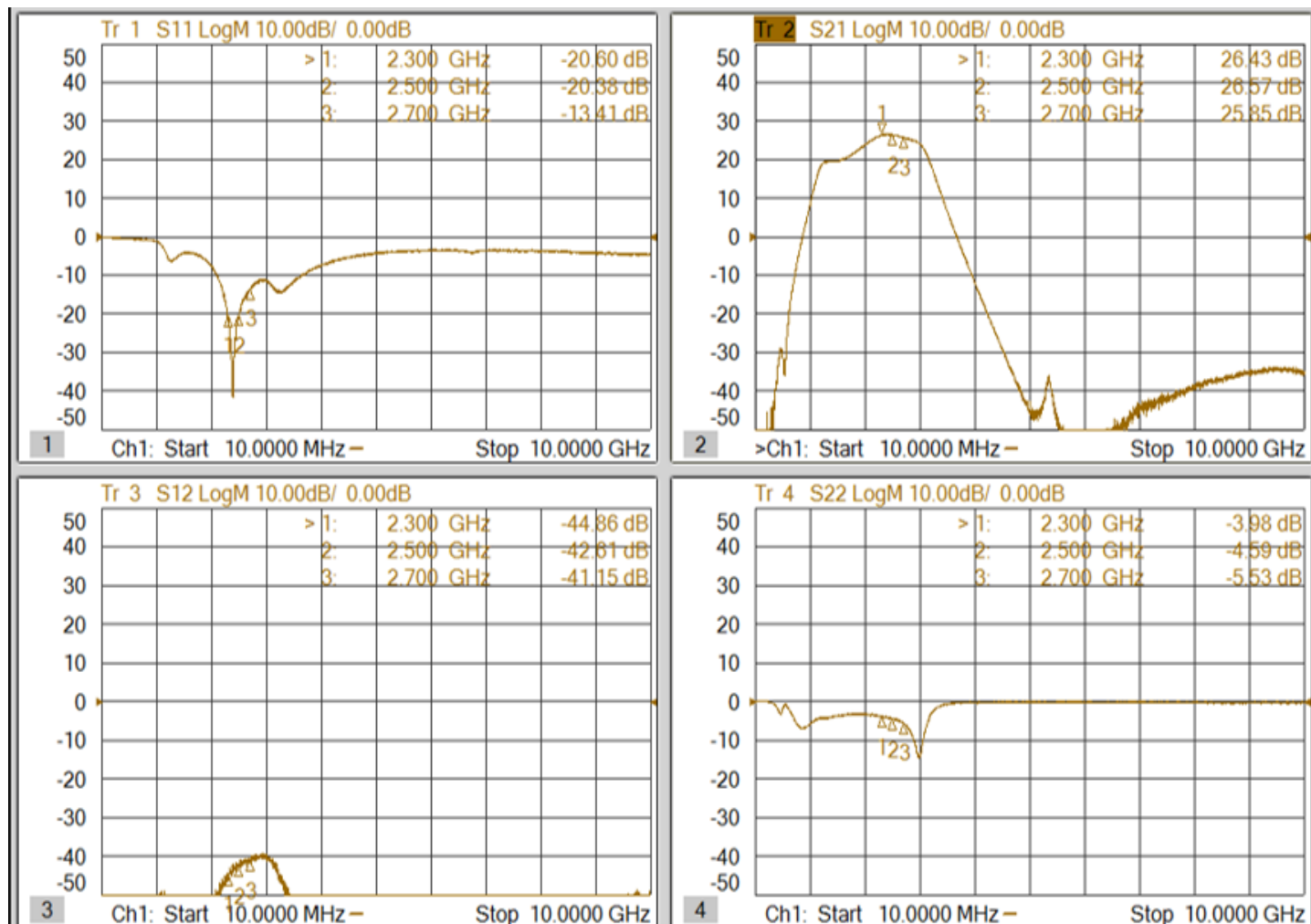
GRF5225 Typical Operating Curves: 2.3 to 2.7 GHz Tune (Modulated with DPD)
GRF5225 ACLR1 vs Pout Modulation 5G_8.2_1x100MHz

GRF5225 ACLR2_Max(dBc) vs Pout Modulation 5G_8.2_1x100MHz


GRF5225 Typical Operating Curves: 2.3 to 2.7 GHz Tune (Modulated with DPD)

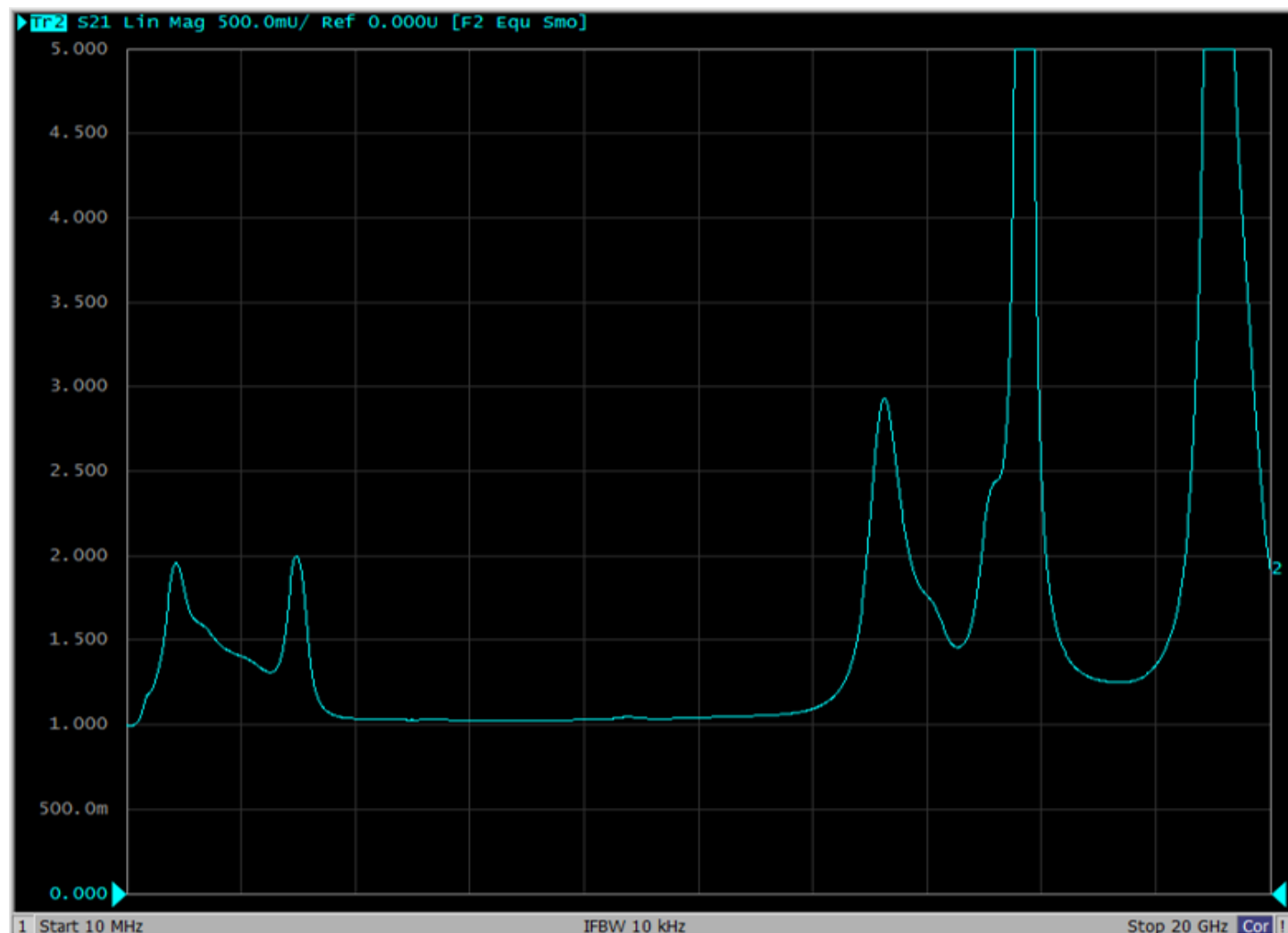


GRF5225 Typical Operating Curves: 2.3 to 2.7 GHz Tune (Modulated with DPD)

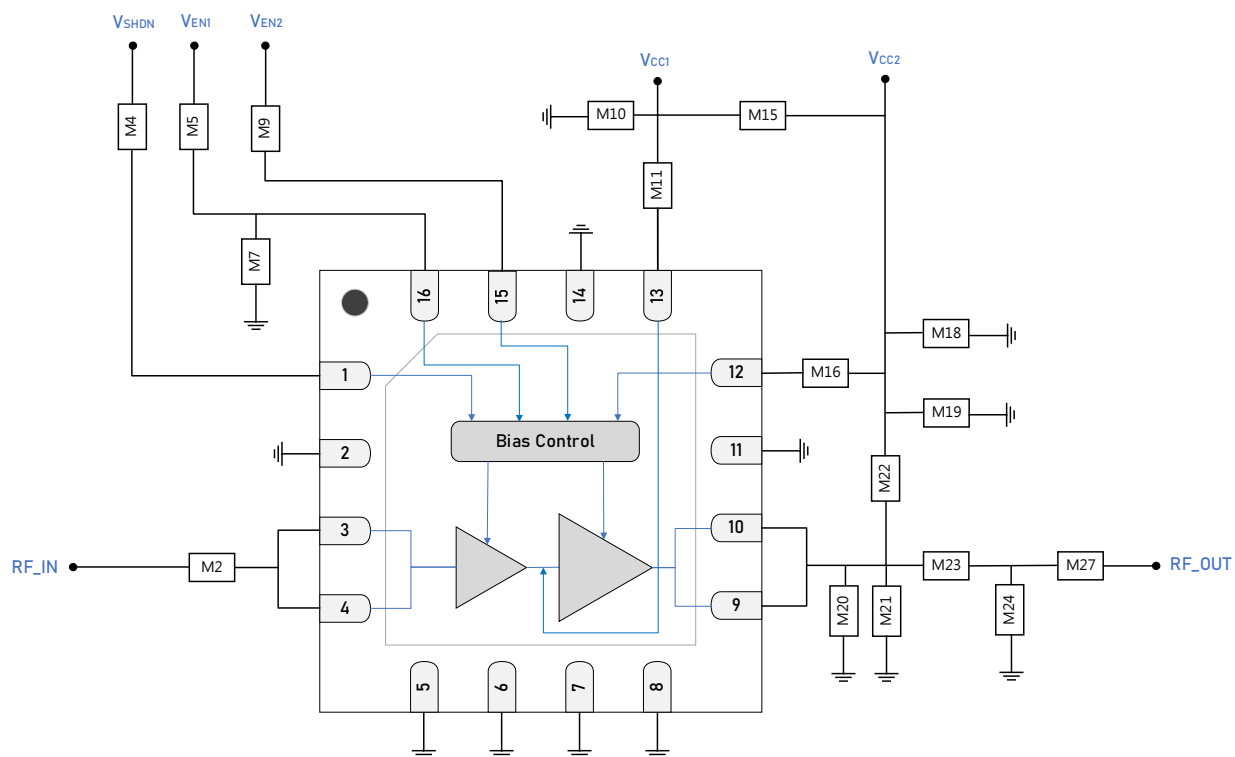


GRF5225 Typical Operating Curves: S-Parameters (2.3 to 2.7 GHz Tune)


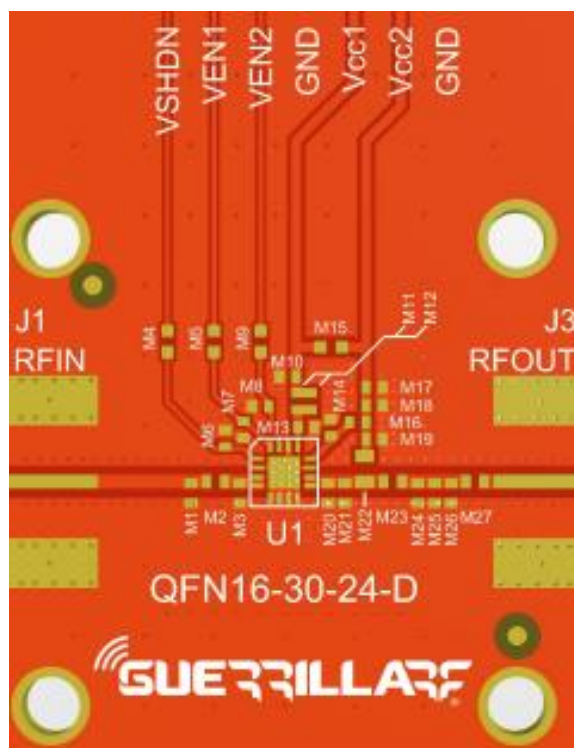
GRF5225 Typical Operating Curves: Stability Mu Factor (10 MHz to 20 GHz)



Note: $\mu \geq 1.0$ implies unconditional stability



GRF5225 Standard Evaluation Board Schematic



GRF5225 Evaluation Board Assembly Diagram

GRF5225 Evaluation Board Assembly Diagram Reference: 2.3 to 2.7 GHz Tune

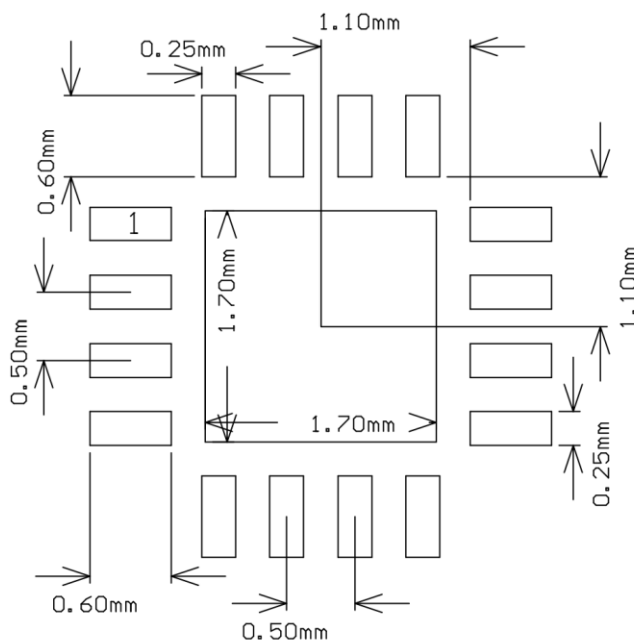
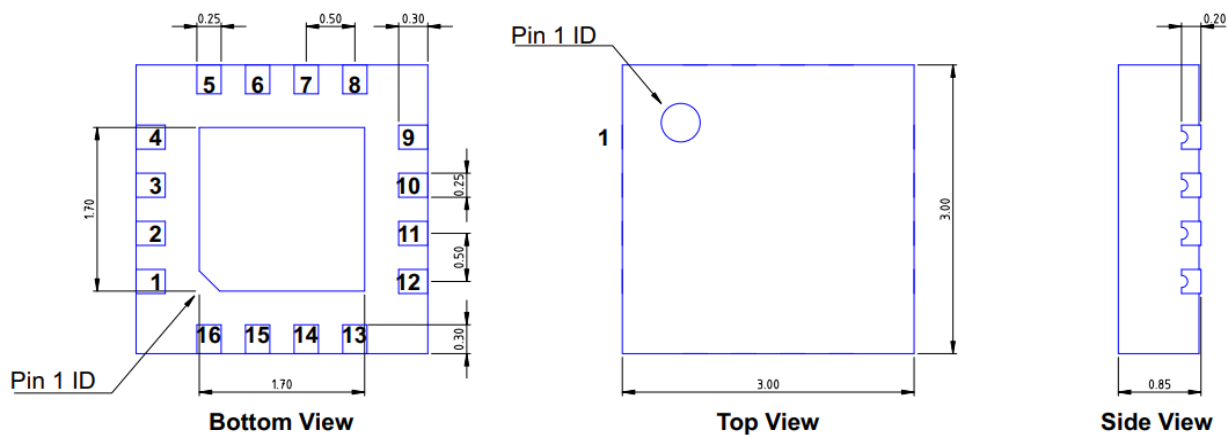
Component	Type	Manufacturer	Family	Value	Package Size	Substitution
M2, M4, M15, M16	Resistor	Various	5%	0 Ω	0402	ok
M5	Resistor	Various	1%	3.0 k Ω	0402	ok
M9	Resistor	Various	1%	3.83 k Ω	0402	ok
M10, M18	Capacitor	Murata	GRM	** 10 μ F	0402	ok
M11	Inductor	Murata	LQGWH	1.3 nH	0402	ok
M19	Capacitor	Murata	GRM	100 pF	0402	ok
*** M20, M21	Capacitor	Murata	GJM	2.5 pF	0402	ok
M22	Inductor	Murata	LQW18AN	3.0 nH	0603	ok
M23	Inductor	Murata	LQGWH	1.2 nH	0402	ok
M24	Capacitor	Murata	GJM	1.6 pF	0402	ok
M27	Capacitor	Murata	GJM	6.8 pF	0402	ok
Evaluation Board	QFN16-30-24-D					

Notes:

Standard evaluation board bias: $V_{CC} = 4$ V, $V_{ENABLE} = 4$ V.

** 10 μ F must be rated for > 4 V at maximum ambient temperature. Manufacturer Part Number in this case = GRM155C80J106ME11D.

*** M20 must be 50 mils from pin. M21 must be 80 mils from pin.


3 x 3 mm QFN-16 Suggested PCB Footprint (Top View)


QFN16 3x3mm
 Dimensions in millimeters
 Dimensional Tolerance: ± 0.05

3 x 3 mm QFN-16 Package Dimensions

Package Marking Diagram



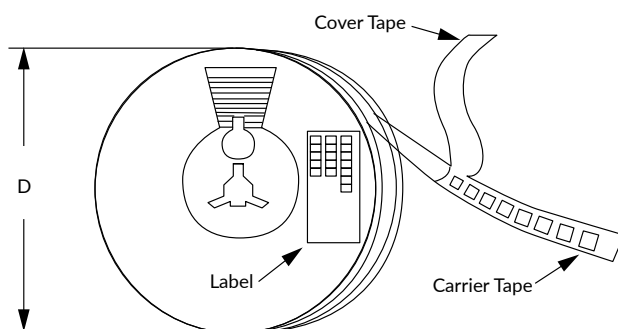
- Line 1: "YY" = YEAR. "WW" = WORK WEEK the device was assembled.
- Line 2: "GRF" = Guerrilla RF.
- Line 3: "XXXX" = Device PART NUMBER.

Tape and Reel Information

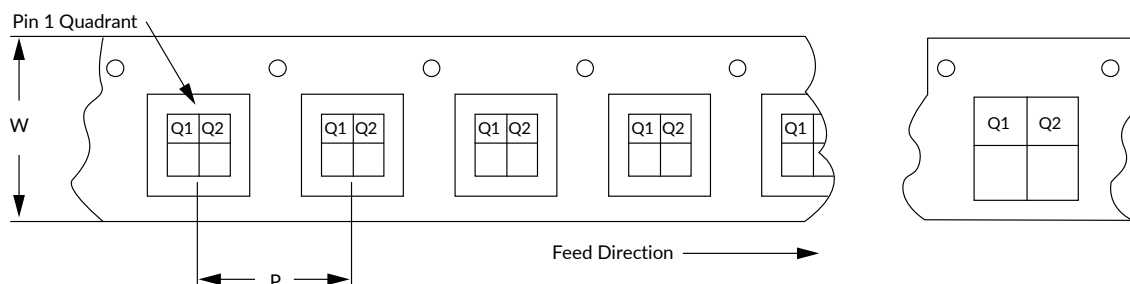
Guerrilla RF's tape and reel specification complies with Electronic Industries Alliance (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). See the following page for the Tape and Reel Specification and Device Package Information table, which includes units per reel.

Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag and the outside surface of the box.

For the Tape and Reel Reference Table, please refer to: <https://www.guerrilla-rf.com/prodFiles/Manufacturing/MN001.pdf>



Tape and Reel Packaging with Reel Diameter Noted (D)



Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information



Revision History

Revision Date	Description of Change
January 23, 2025	Preliminary Data sheet.



Datasheet Classifications

Data Sheet Status	Notes
Advance	S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices.
Preliminary	All data based on limited evaluation board measurements taken within the Guerrilla RF Applications Lab. All parametric values are subject to change pending the collection of additional data.
Release Ø	All data based on measurements taken with <i>production-released</i> material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using <i>modelled estimates</i> that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory.
Release A-Z	All data based on measurements taken with production-released material <i>derived from multiple lots which have been fabricated over an extended period of time</i> . MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads.

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