DATA SHEET

GRF5536

HIGH LINEARITY POWER AMPLIFIER
3.3 to 4.2 GHz

RELEASE A DATA SHEET

FEATURES

- Excellent OP1dB, OIP3, ACLR and IM3 Performance
- Native Linearity Provides up to +23 dBm P_{OUT} with > 45 dBc ACLR – Without the Need for Digital Predistortion Correction
- +23 dBm Linear Output Power Maintained at 105 °C
- Flexible Biasing Provides Latitude for Linearity Optimization
- 205 mA Native Mode Quiescent Current Consumption
- 5 V Supply Voltage
- 50 Ω Single-ended Input and Output Impedances
- Digital Shutdown
- Rugged Design is Extremely Resilient to Mismatched Loads
- -40 to 105 °C Operating Temperature Range
- Compact 3 x 3 mm QFN-16 Package

Reference: 5 V / 205 mA I_{CCQ} / 3.55 GHz

- Gain: 24.8 dB
- OIP3: 47.8 dBm @ 23 dBm $P_{OUT/tone}$
- OP1dB: 32.6 dBm
- Noise Figure: 4.1 dB

APPLICATIONS

- Cellular Boosters/Repeaters
- Automotive Compensators
- Picocells/Femtocells
- Cellular DAS
- Customer Premises Equipment
- Wireless Infrastructure

ORDERING INFORMATION

Buy it Now

DESCRIPTION

The GRF5536 is a high gain, two-stage InGaP HBT power amplifier designed to deliver excellent P1dB, ACLR and IM3 performance over the standard 3.3 to 3.8 GHz band. Its exceptional native linearity makes it an ideal choice for transmitter applications that typically do not employ digital predistortion correction schemes.

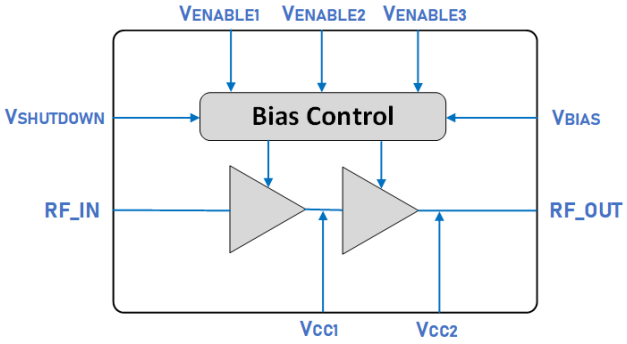
An extended bandwidth tune covering 3.3 to 4.2 GHz is available. Additional tunes can be found on the GRF5536 "Custom Tunes" product page: GRF5536 Custom Tunes

This device is part of a complete family of externally matched linear amplifiers that cover the following frequency ranges:

GRF5506: 0.66 - 0.72 GHz	GRF5518: 1.8 - 2.0 GHz
GRF5507: 0.7 - 0.91 GHz	GRF5519: 1.92 - 2.2 GHz
GRF5508: 0.777 - 0.96 GHz	GRF5521: 2.11 - 2.17 GHz
GRF5510: 0.88 - 0.96 GHz	GRF5526: 2.2 - 2.7 GHz
GRF5517: 1.6 - 1.92 GHz	GRF5536: 3.3 - 4.2 GHz

Please consult with the GRF applications engineering team for custom tuning/evaluation board data.

BLOCK DIAGRAM



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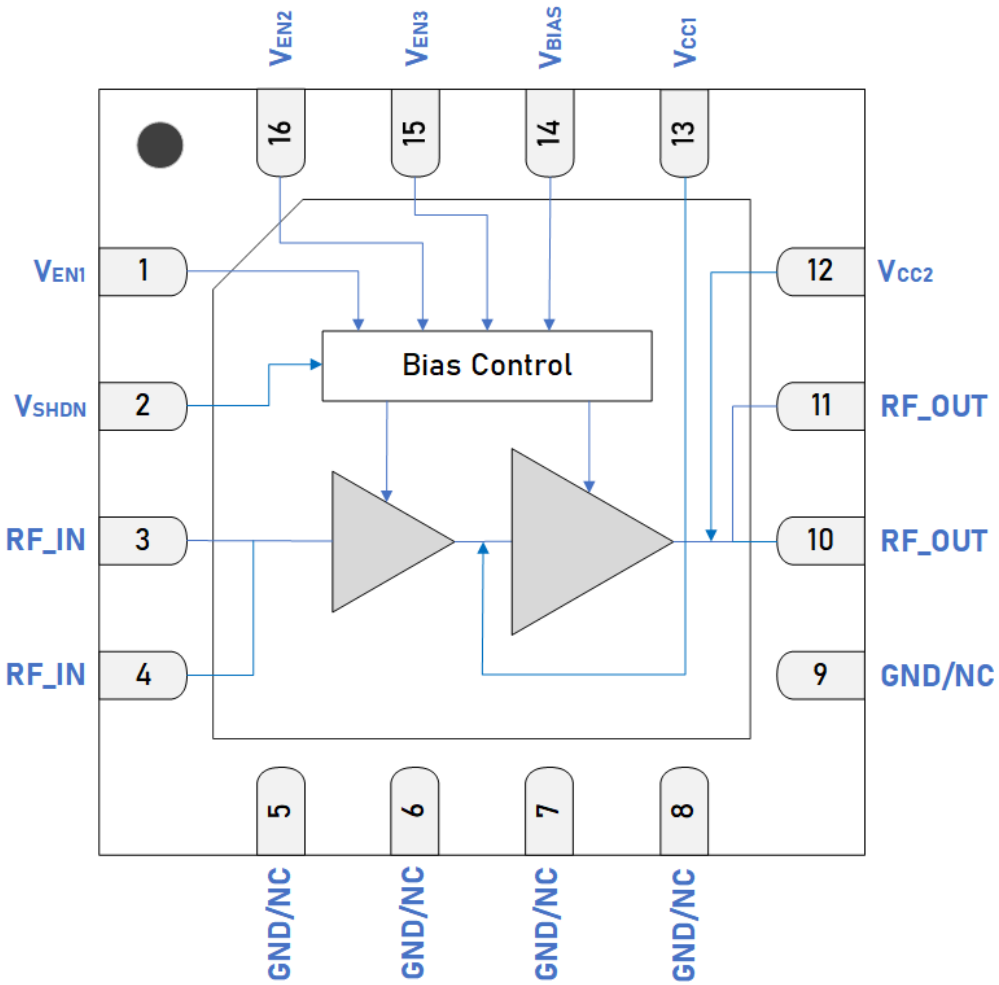


Pin Out (Top View)

Pin Assignments

Pin	Name	Description	Note
1	V_{EN1}	Enable1 Voltage Input	V_{EN1} and series resistor sets I_{CCQ} for the output stage. $V_{EN1} \leq$ 0.2 volts disables stage 1.
2	V_{SHDN}	Digital Shutdown Pin	$V_{SHDN} \geq$ 1.7 V (Logic HIGH) disables device. $V_{SHDN} \leq$ 0.9 V (Logic LOW) enables device.
3, 4	RF_IN	RF Input	Pins 3 & 4 tied together on system board. An external DC blocking cap must be used.
5, 6, 7, 8, 9	GND/NC	Ground or No Connect	No internal connection to die. These pins can be left unconnected, or be connected to ground (recommended). Use a via as close to the pin as possible if grounded.
10, 11	RF_OUT	PA Output	Pins 10 & 11 tied together on system board.
12	V_{CC2}	Bias Voltage	V_{CC2} must be applied to this pin via an RF choke.
13	V_{CC1}	Bias Voltage	V_{CC1} must be applied to this pin via L-C interstage match.
14	V_{BIAS}	Bias Circuit Supply	Connect to V_{CC2} through an external resistor.
15	V_{EN3}	Enable3 Voltage Input	Bias Voltage applied via series resistor.
16	V_{EN2}	Enable2 Voltage Input	V_{EN2} and series resistor set I_{CCQ} for the output stage. $V_{EN2} \leq$ 0.2 V disables stage 2.
PKG BASE	GND	Ground	Provides DC and RF ground for the amplifier, as well as thermal heat sink. Recommend multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page.

Note 1: GRF5526 and GRF5536 have a common pinout that is slightly different from the pinout shared by all the other GRF55XXW PAs. Please see page 2.

Absolute Ratings

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage		V_{CC}	4	5.5	V
RF Input Power	50 Ω, V_{CC} = 5 V, CW Tone, 100% Duty Cycle, $T_{PKG\ BASE}$ = 25°C.	$P_{IN\ MAX}$ - 1:1		20	dBm
	Load VSWR ≤ 8:1, all phase angles, V_{CC} = 5 V, CW Tone, 100% Duty Cycle, $T_{PKG\ BASE}$ = -40 to 105°C.	$P_{IN\ MAX}$ - 8:1		17	
Operating Temperature (Package Base).		$T_{PKG\ BASE}$	-40	105	°C
Maximum Junction Temperature (MTTF >10^6 Hours).		$T_{J\ MAX}$		170	°C
Maximum Dissipated Power (Stage 1). DC only. No RF applied.		$P_{DISS\ MAX}$		* 360	mW
Maximum Dissipated Power (Stage 2). DC only. No RF applied.		$P_{DISS\ MAX}$		* 1250	mW
Shutdown Voltage		V_{SHDN}		** 5.5	V

* Bias resistors M2/M4 have been empirically optimized for linearity. Thus, there will be no benefit in decreasing resistance (thereby increasing I_{CCQ}).

** With M1 = 0 Ω, I_{SHDN} increases linearly from V_{SHDN}/I_{SHDN} = 1.8V/82µA to 4.2V/498µA.

Said linear relationship can be used to scale M1 for higher V_{SHDN} voltage: use pin condition V_{SHDN_pin}/I_{SHDN} = 2.2V/146µA.

Calculate M1 for V_{SHDN}/I_{SHDN} = 5V/146µA: M1 = (5–2.2)/(0.000146) = 19.2 kΩ.

Absolute Ratings (continued)

Electrostatic Discharge

Human Body Model	HBM	1000		V

Storage

Storage Temperature	T_{STG}	-65	150	°C
Moisture Sensitivity Level	MSL		1	--

Caution! ESD Sensitive Device.

Exceeding Absolute Maximum Rating conditions may cause permanent damage.

Note: For additional information, please refer to Manufacturing Note MN-001 - Packaging and Manufacturing Information.

All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging. For additional information, please refer to the Certificate of RoHS Compliance.

Recommended Operating Conditions

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4	5	5.5	V	
Operating Temperature (Package Base)	$T_{PKG\ BASE}$	-40		105	°C	
RF Frequency Range	F_{RF}	3.3		3.8	GHz	Typical application schematic using the 3.3 to 3.8 GHz tuning set **(notes 2 & 3)**.
	F_{RF}	3.3		4.2	GHz	Typical application schematic using the 3.3 to 4.2 GHz tuning set **(notes 2 & 3)**.
RF_IN Port Impedance	Z_{RFIN}		50		Ω	Single ended with 2-element match.
RF_OUT Port Impedance	Z_{RFOUT}		50		Ω	Single ended with 2-element match.

Note 2: Operation outside of this range is supported by using different custom tunes. Examples of other optimized tunes can be found here: GRF5536 Custom Tunes

Note 3: Contact the Guerrilla RF Applications team for guidance of optimizing the tuning of the device for alternative bands.

Nominal Operating Parameters - General

The following conditions apply unless noted otherwise: typical application schematic using the 3.3 to 3.8 GHz tuning set. M2 = 6040 Ω, M4 = 3570 Ω, M10 = 1200 Ω, V_{SHDN} = LOW, V_{CC} = +4.75 to +5.25 V, I_{CCQ} = 205 mA, P_{OUT} = +23 dBm, F_{TEST} = 3.55 GHz, $T_{PKG\ BASE}$ = -40 to +105 °C. Typical values: V_{CC} = 5 V, I_{CCQ} = 205 mA, P_{OUT} = +23 dBm, F_{TEST} = 3.55 GHz, $T_{PKG\ BASE}$ = 25 °C. 50 Ω system impedance, Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Supply Quiescent Current	I_{CCQ}		205		mA	I_{CCQ1} + I_{CCQ2}. No RF applied.
Supply Current with RF Applied	I_{CC}		280		mA	I_{CC1} + I_{CC2}. RF applied. P_{OUT} = 23 dBm.
Enable Current 1	$I_{ENABLE1}$		0.18		mA	V_{CC} = 5 V, $T_{PKG\ HEAT\ SINK}$ = 25 °C.
Enable Current 2	$I_{ENABLE2}$		0.49		mA	V_{CC} = 5 V, $T_{PKG\ HEAT\ SINK}$ = 25 °C.
Enable Current 3	$I_{ENABLE3}$		0.8		mA	V_{CC} = 5 V, $T_{PKG\ HEAT\ SINK}$ = 25 °C.
Operating Temperature Range	$T_{PKG\ BASE}$	-40		105	°C	Measured on Package Base.
Logic Input Low	V_{IL}	0		0.9	V	Applies to V_{SHDN} Input.
Logic Input High	V_{IH}	1.7		V_{CC}	V	Applies to V_{SHDN} Input.
Logic Current Low	I_{IL}		3		nA	Applies to V_{SHDN} Input. V_{IL} = 0.9 V.
Logic Input High	I_{IH}		82		µA	Applies to V_{SHDN} Input. V_{IH} = 1.8 V.
			322			Applies to V_{SHDN} Input. V_{IH} = 3.3 V.
Switching Rise Time	T_{RISE}		150		ns	Applies to V_{SHDN} Input.
Switching Fall Time	T_{FALL}		10		ns	Applies to V_{SHDN} Input.

Disabled Mode

Supply Quiescent Current	$I_{CCQ-SHDN}$		240		µA	V_{CC} = 5 V, V_{SHDN}/V_{EN1}/V_{EN3} = HIGH
Enable Current 1	$I_{ENABLE1-SHDN}$		0.5		mA	V_{CC} = 5 V, V_{SHDN}/V_{EN1}/V_{EN3} = HIGH
Enable Current 2	$I_{ENABLE2-SHDN}$		1.1		mA	V_{CC} = 5 V, V_{SHDN}/V_{EN1}/V_{EN3} = HIGH
Enable Current 3	$I_{ENABLE3-SHDN}$		3.3		mA	V_{CC} = 5 V, V_{SHDN}/V_{EN1}/V_{EN3} = HIGH

Thermal Data

See plot of Junction Temperature vs. Output Power.						On standard evaluation board.

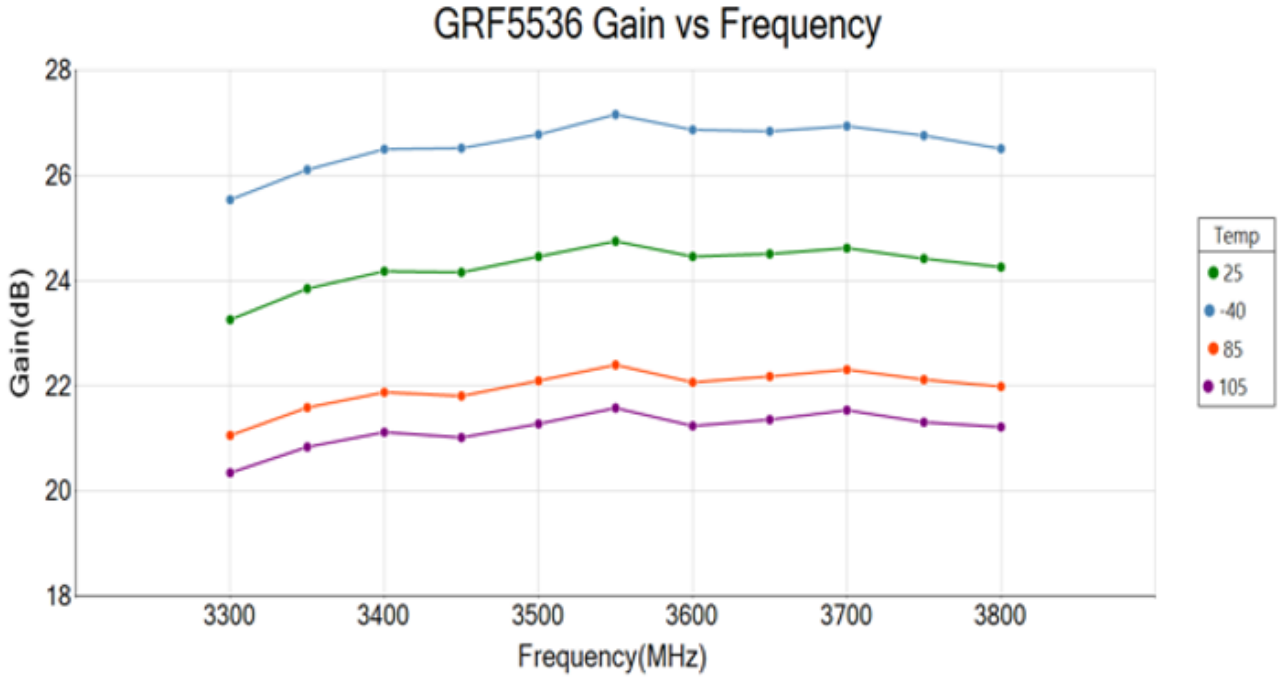
Nominal Operating Parameters - RF

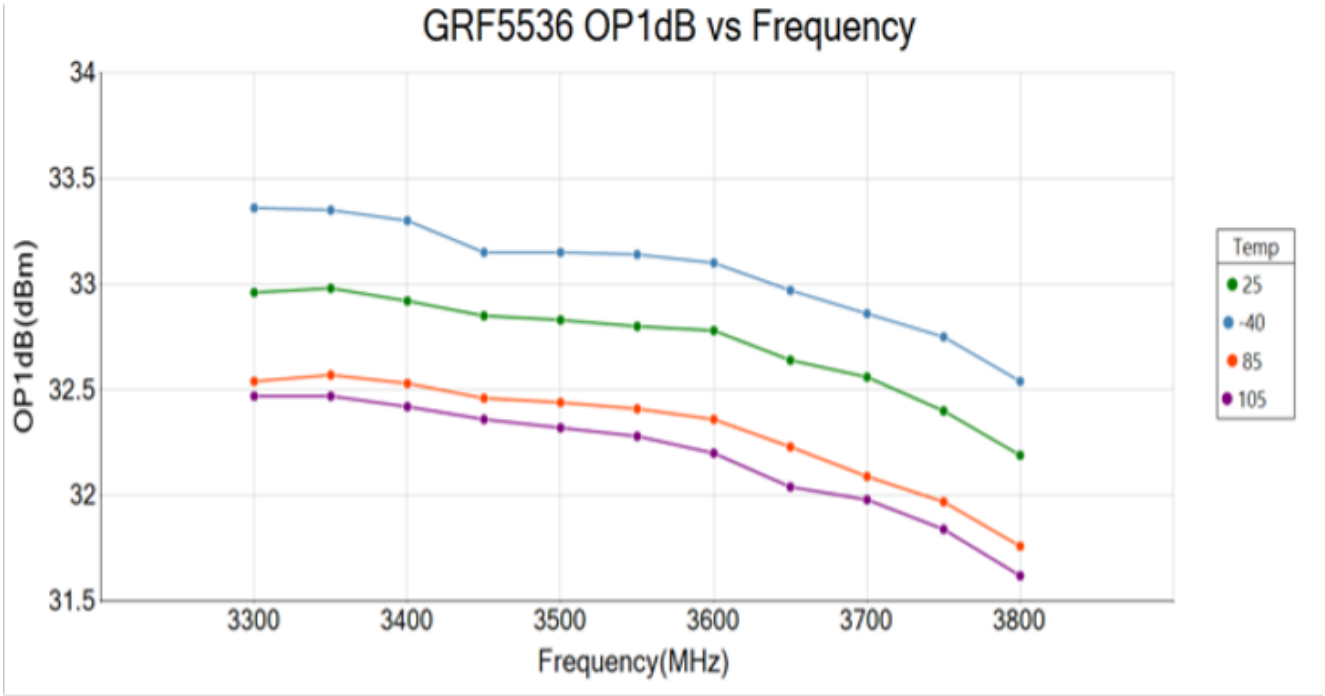
The following conditions apply unless noted otherwise: Typical Application Schematic using the 3.3 to 3.8 GHz tuning set. M2 = 6040 Ω, M4 = 3570 Ω, M10 = 1200 Ω, V_{SHDN} = LOW, V_{CC} = +4.75 to +5.25 V, I_{CCQ} = 205 mA, P_{OUT} = +23 dBm, F_{TEST} = 3.55 GHz, $T_{PKG\ BASE}$ = -40 to +105 °C. Typical values: V_{CC} = 5 V, I_{CCQ} = 205 mA, P_{OUT} = +23 dBm, F_{TEST} = 3.55 GHz, 50 Ω system impedance, $T_{PKG\ BASE}$ = 25 °C. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Small Signal Gain	S21	22.5	24.8		dB	LTE 20MHz 100RB TM1.1 Downlink Waveform with 9.8 dB PAR, F_{TEST} = 3.6 GHz, $T_{PKG\ BASE}$ = 25 °C, V_{CC} = 5 V, P_{IN} = -25 dBm.
Standby Mode Gain	$S21_{STBY}$		-45		dB	Disabled Mode, LTE 20MHz 100RB TM1.1 Downlink Waveform with 9.8 dB PAR, $V_{SHDN}/V_{EN1}/V_{EN2}$ = HIGH, P_{IN} = 0 dBm.
Input Return Loss	S11		< -2		dB	F_{RF} = 3.3 to 3.8 GHz.
Output Return Loss	S22		< -4		dB	F_{RF} = 3.3 to 3.8 GHz.
Reverse Isolation	S12		< -34		dB	F_{RF} = 3.3 to 3.8 GHz.
Noise Figure	NF		4.1		dB	On standard evaluation board.
Output 3rd Order Intercept Point	OIP3		47.8		dBm	+23 dBm P_{OUT} per tone at 600 kHz spacing.
Output 1 dB Compression Power	OP1dB		32.8		dBm	Sine wave input, V_{CC} = 5 V, $T_{PKG\ BASE}$ = 25 °C.
2nd Harmonic	$2f_0$			-22	dBc	P_{OUT} = 26 dBm **(note 4)**.
3rd Harmonic	$3f_0$			-45	dBc	P_{OUT} = 26 dBm **(note 4)**.
Adjacent Channel Leakage Ratio	ACLR		-48		dBc	P_{OUT} = +23 dBm. LTE 20MHz 100RB TM1.1 Downlink Waveform with 9.8 dB PAR, F_{TEST} = 3.55 GHz, $T_{PKG\ BASE}$ = 25 °C, V_{CC} = 5 V.

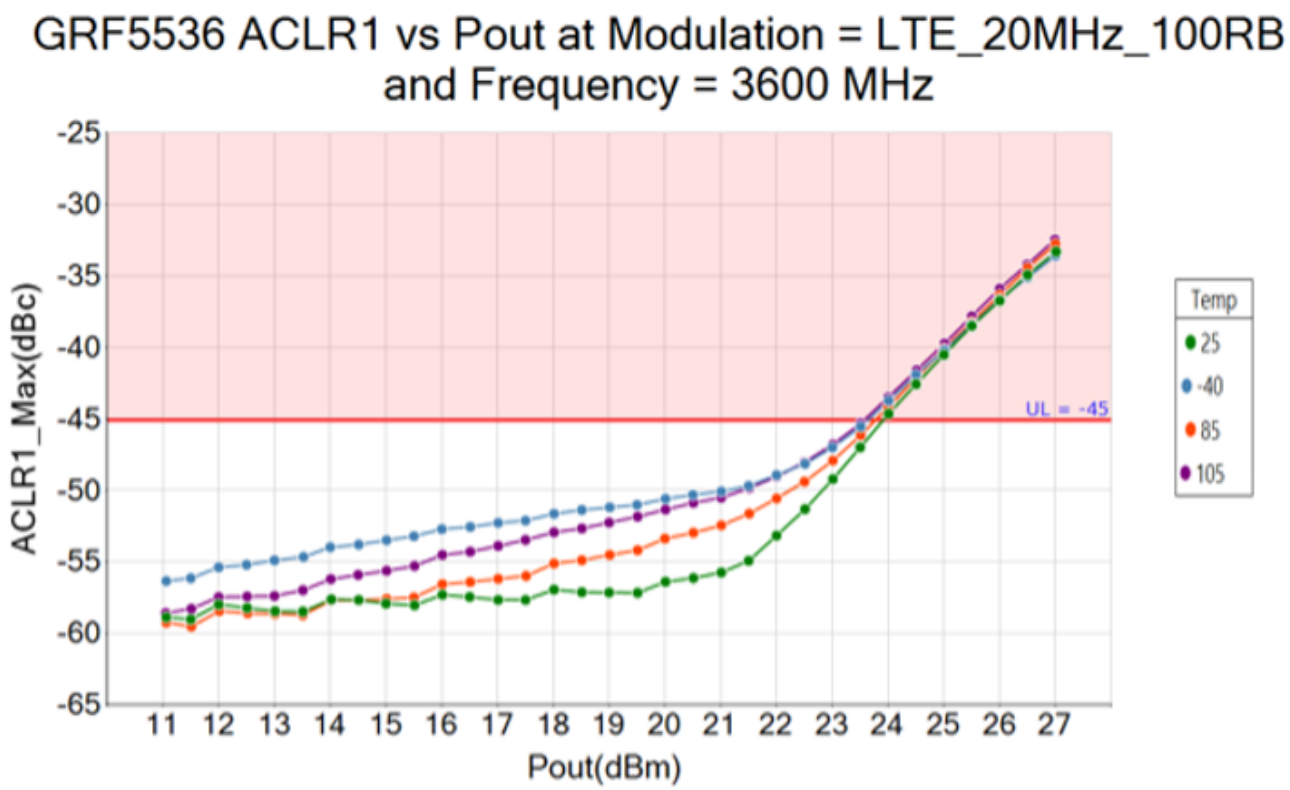
Note 4: MIN/MAX limits defined using ***modeled estimates*** that account for part-to-part variations and expected process spreads. As additional production lots are fabricated, accumulated test data will be used to refine the MIN/MAX limits.

GRF5536 Typical Operating Curves: 3.3 to 3.8 GHz Tune

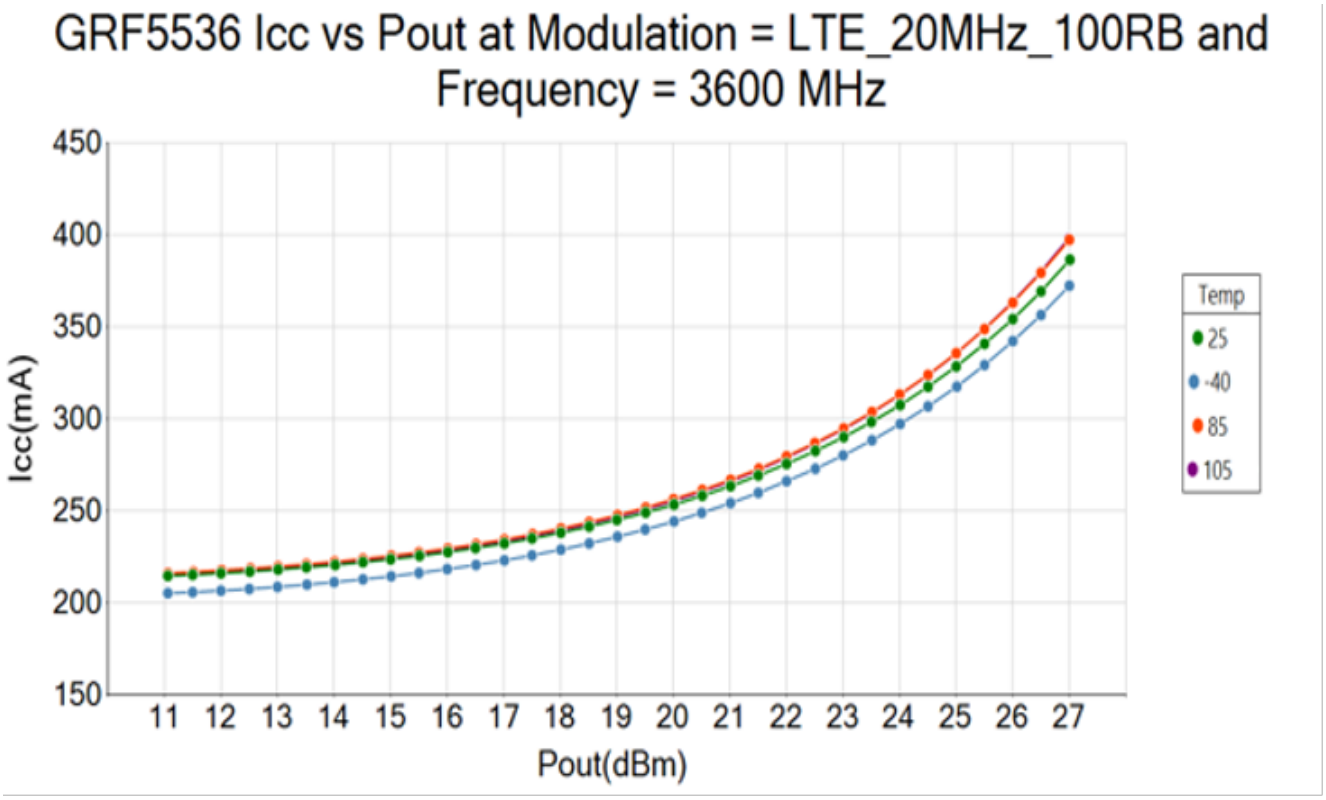




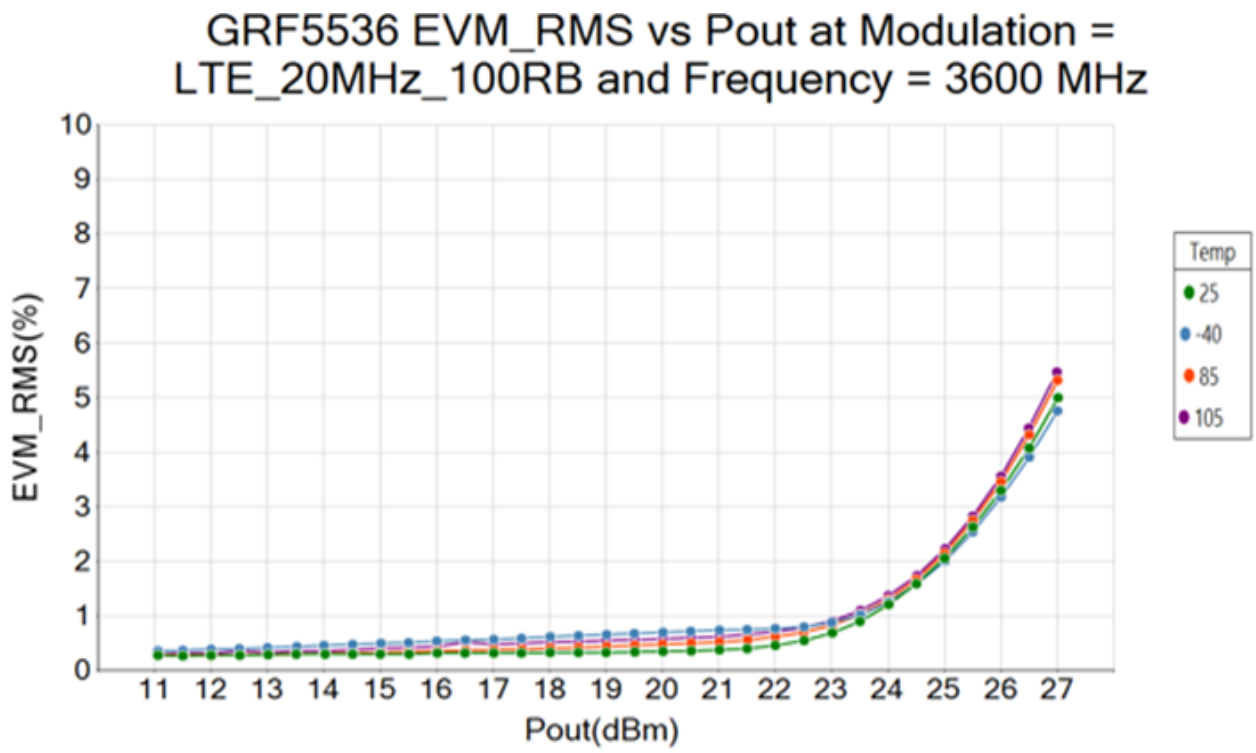
GRF5536 Typical Operating Curves: ACLR vs. P_{OUT} (LTE 20Q100RB TM1.1 9.8 dB PAR)



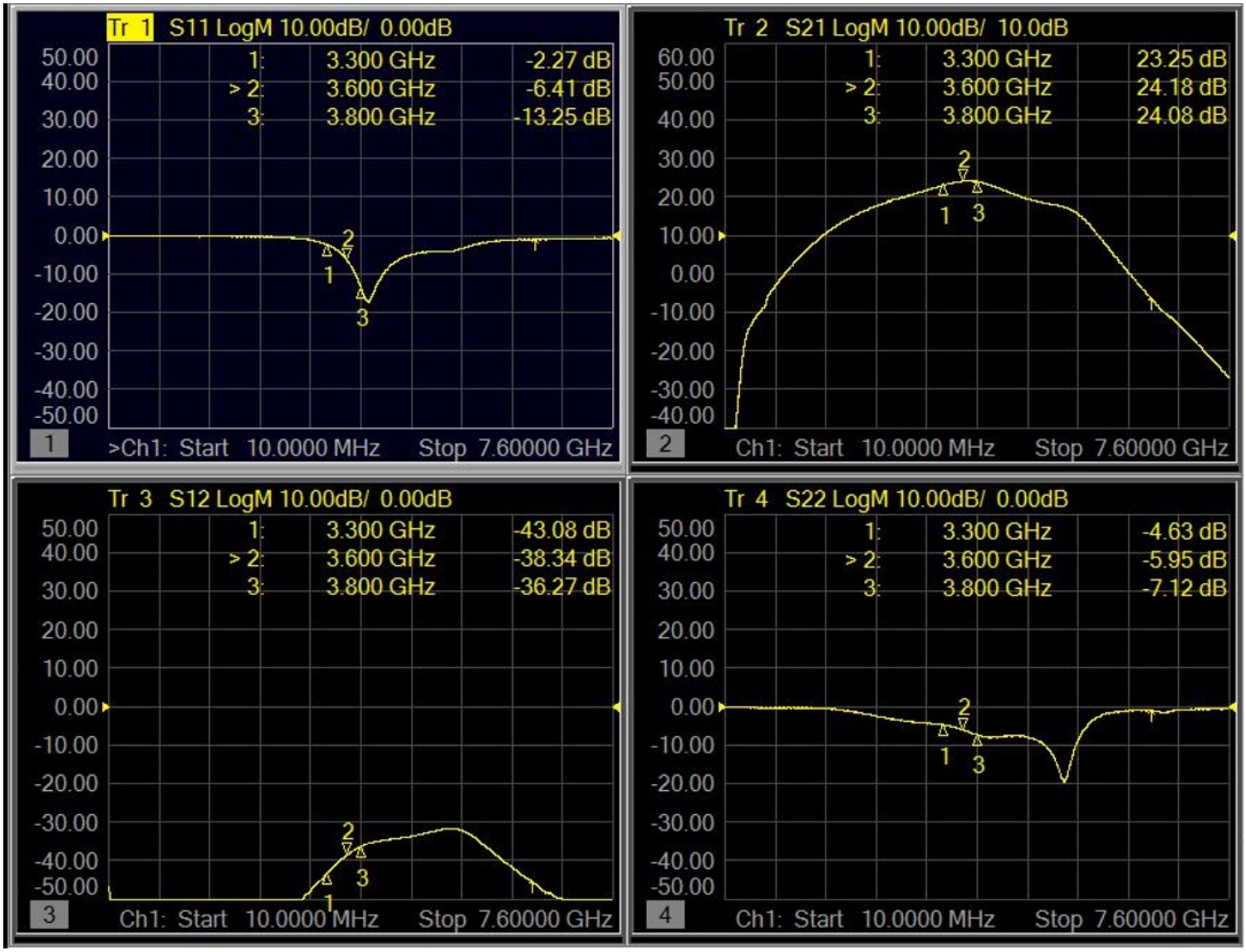
GRF5536 Typical Operating Curves: Stage 1 + Stage 2 I_{CC} vs. P_{OUT} (LTE 20Q100RB TM1.1 9.8 dB PAR)



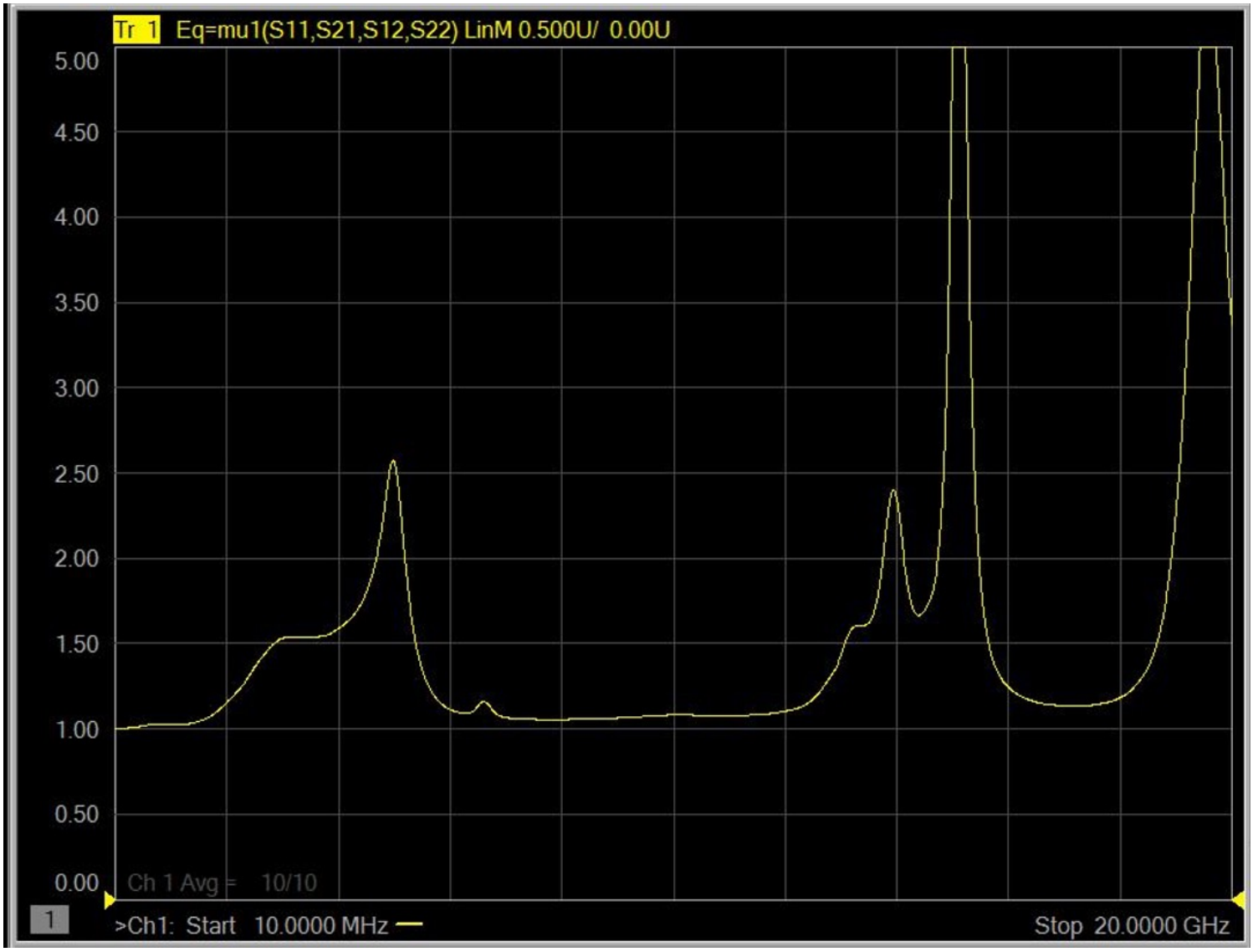
GRF5536 Typical Operating Curves: EVM vs. P_{OUT} (LTE 20Q100RB TM1.1 9.8 dB PAR)



GRF5536 Typical Operating Curves: S-Parameters (3.3 to 3.8 GHz Tune)



GRF5536 Typical Operating Curves: Stability Mu (10 MHz to 20 GHz)

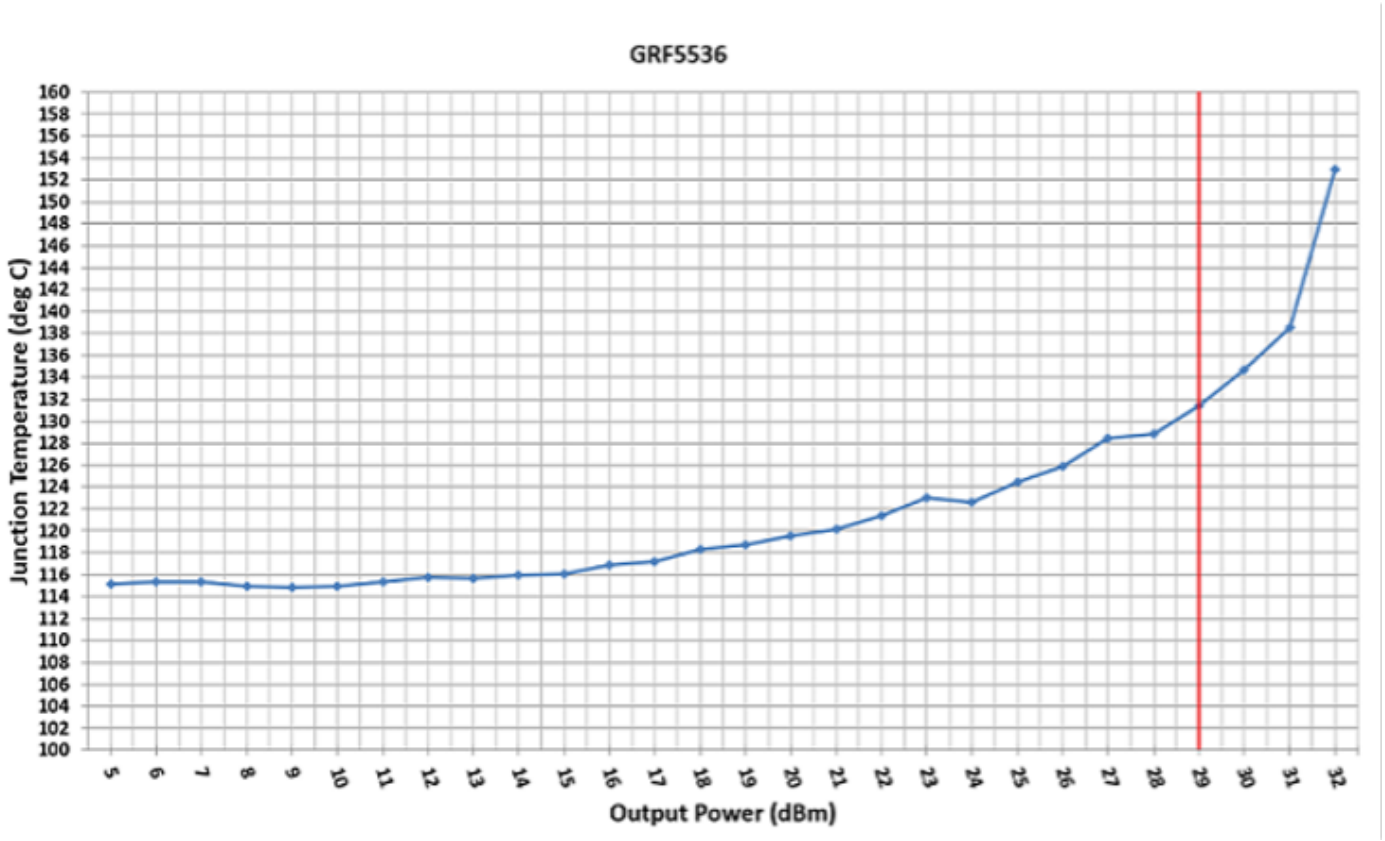


Note: Mu factor ≥ 1.0 implies unconditional stability.

GRF5536 Typical Operating Curves: Junction Temperature (per application schematic @ 85 °C)

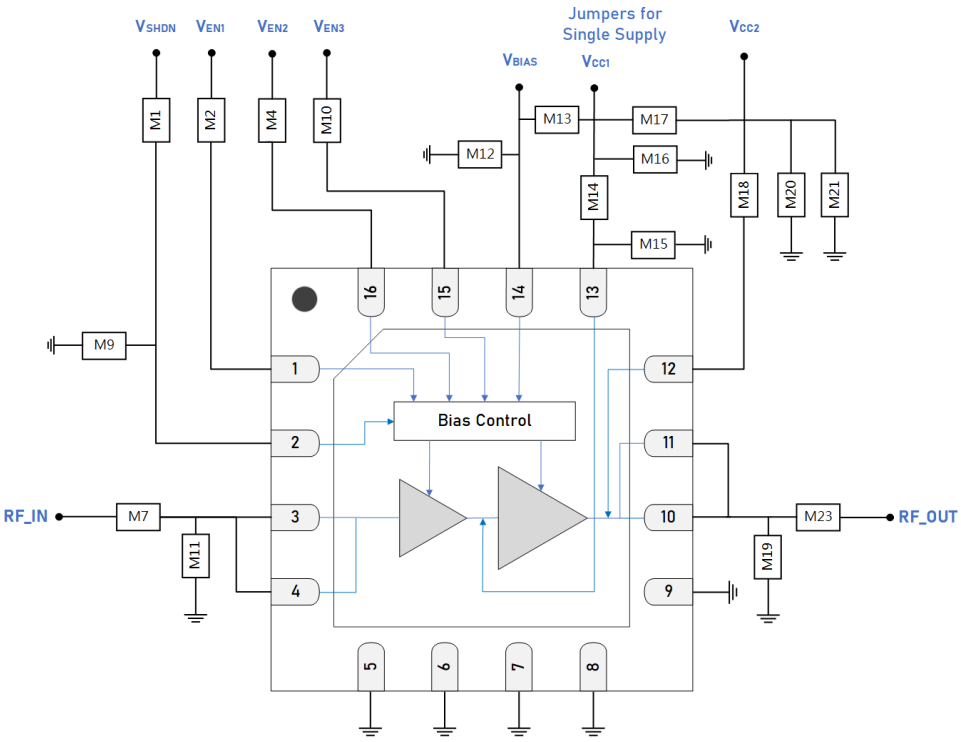
GRF5536, being a 2-stage device, sees one of the stages governing junction temperature over power sweep. Red line = 29 dBm shows where T_J is equivalent in both stages. At left of red line, stage 2 governs T_J (Q2 T_J is higher). To the right of red line, stage 1 governs T_J (Q1 T_J is higher).

Setting bias resistor M2/M4 per application schematic ensures best linearity and yields thermal performance shown in the plot. If the application does not require high IMD3/ACLR linearity, bias resistor can be adjusted higher. This will lower bias point(s) and junction temperature will be contained within/below that shown in the plot.

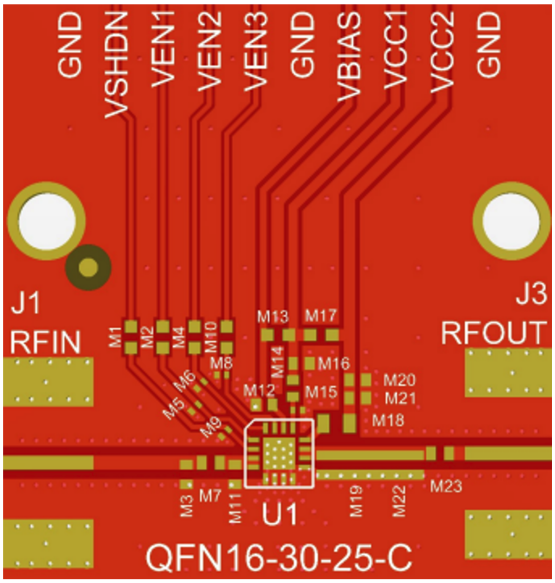


Truth Table

Pin	Logic	Condition
V_{SHDN}	LOW	Full Operation
	HIGH	All Amplifiers Off
V_{EN1}	LOW	Stage 1 Amplifier Off
	HIGH	Stage 1 Amplifier On
V_{EN2}	LOW	Stage 2 Amplifier Off
	HIGH	Stage 2 Amplifier On
V_{EN3}	LOW	Stage 2 Amplifier Off
	HIGH	Stage 2 Amplifier On



GRF5536 Standard Evaluation Board Schematic



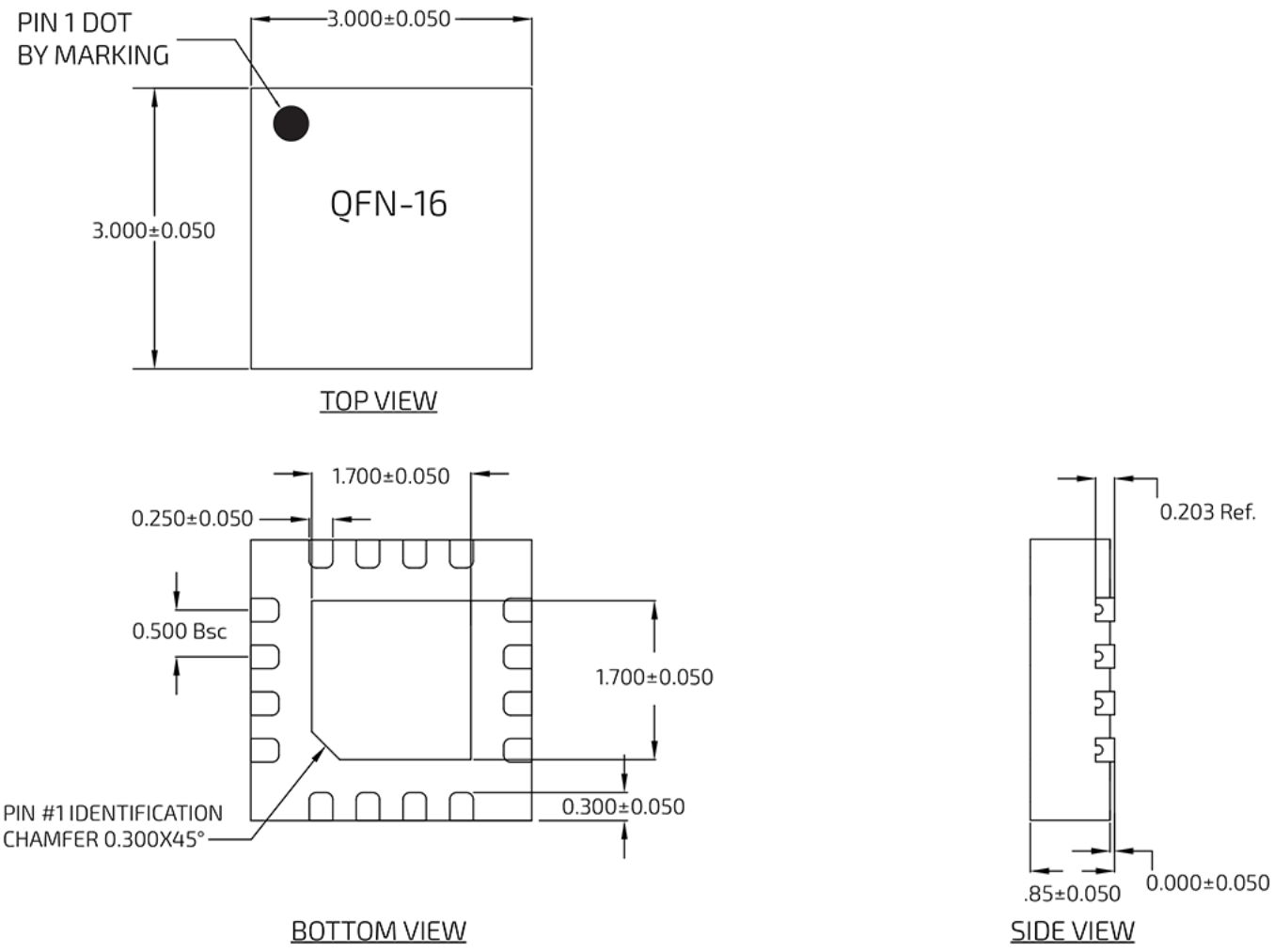
GRF5536 Evaluation Board Assembly Diagram

GRF5536 Evaluation Board Assembly Diagram Reference

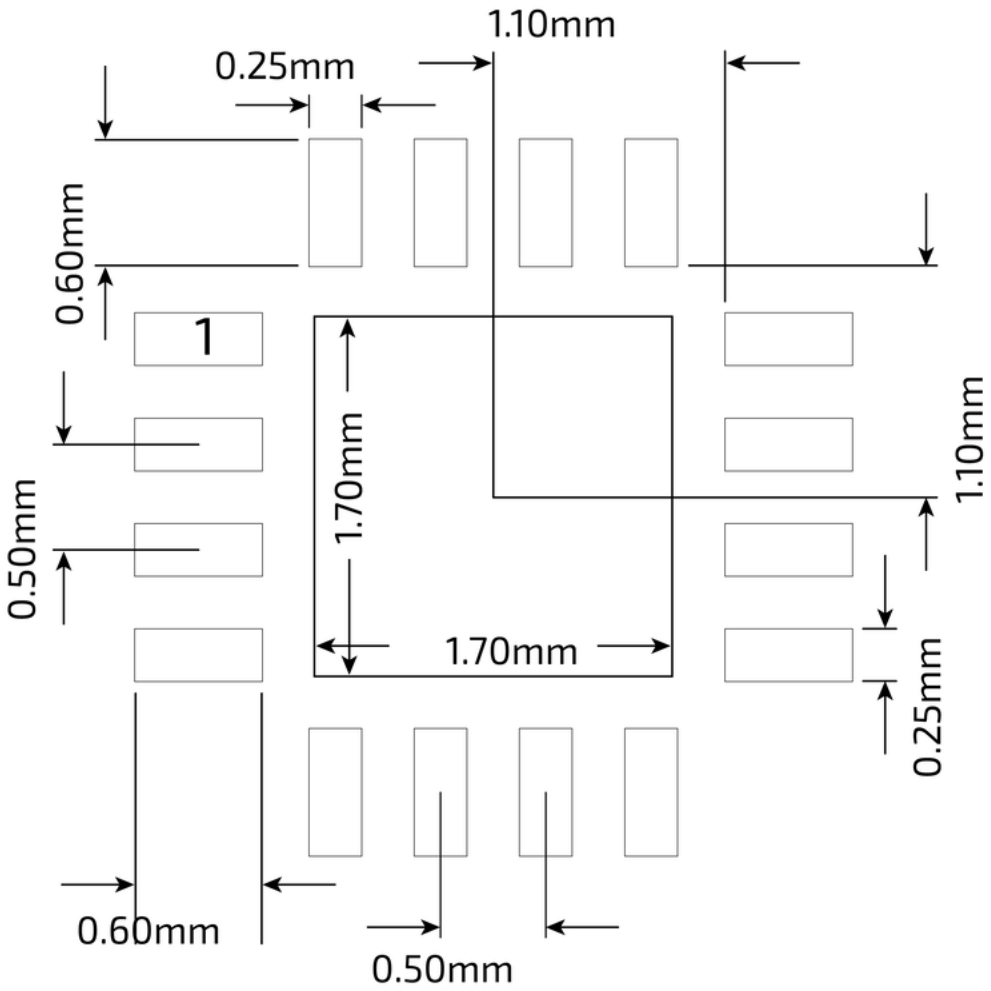
Component	Type	Manufacturer	Family	Value	Package Size	Substitution
M1	Resistor	Various	5%	0 Ω	0402	ok
M2	Resistor	Various	1%	6040 Ω	0402	ok
M4	Resistor	Various	1%	3570 Ω	0402	ok
M7	Capacitor	Murata	GJM	0.7 pF	0402	ok
M9	Capacitor	Murata	GJM	10 pF	0201	ok
M10	Resistor	Various	1%	1200 Ω	0402	ok
M11	Capacitor	Murata	GJM	0.8 pF	0402	ok
M12	Capacitor	Murata	GRM	** 10 µF	0402	ok
M13	Resistor (jumper)	Various	5%	0 Ω	0402	ok
M14	Resistor	Various	5%	0 Ω	0402	ok
M15	Capacitor	Murata	GRM	0.1 µF	0201	ok
M16	Capacitor	Murata	GRM	** 10 µF	0402	ok
M17	Resistor (jumper)	Various	5%	0 Ω	0402	ok
M18	Inductor	Murata	LQW	10 nH	0402	ok
M19	Capacitor	Murata	GJM	0.8 pF	0402	ok
M20	Capacitor	Murata	GRM	10 µF	0402	ok
M21	Capacitor	Murata	GRM	100 pF	0402	ok
M23	Capacitor	Murata	GJM	10 pF	0402	ok
Evaluation Board	QFN16-30-25-C					

Note 5: Standard evaluation board bias: V_{CC} = 5 V, V_{ENABLE} = 5 V.

** GRM155C80J106ME11D rated for 5 V @ 105 ºC.



QFN 16 3x3mm Package Dimensions



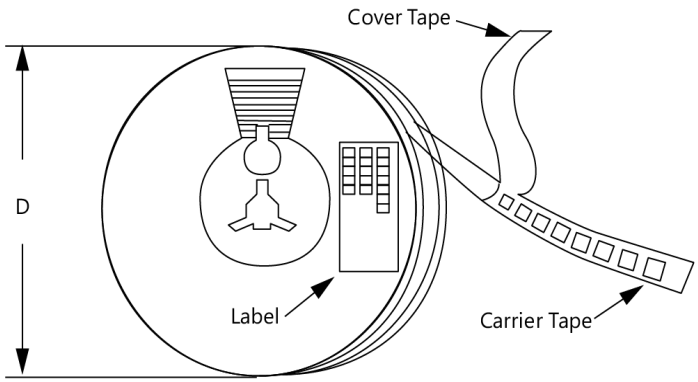
QFN 16 3x3mm Suggested PCB Footprint (Top View)

Package Marking Diagram

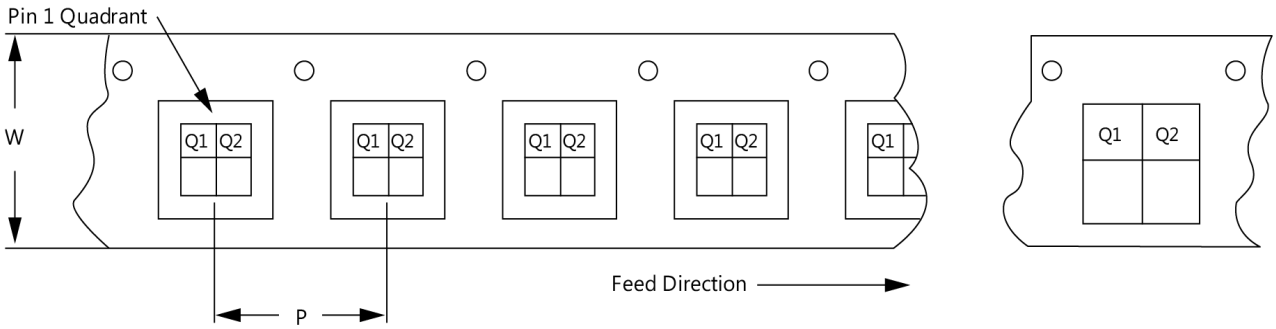
Line 1: “YY” = Year. “WW” = WORK WEEK the Device was assembled.
Line 2: “GRF” = Guerrilla RF
Line 3: “XXXX” = Device Part Number.

Tape and Reel Information

Guerrilla RF's tape and reel specification complies with Electronics Industries Association (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag, and the outside surface of the box. For the latest reel specifications and package information (including units/reel), please visit Package Manufacturing Information | Guerrilla RF (guerrilla-rf.com).



Tape and Reel Packaging with Reel Diameter Noted (D)



Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information

Revision History

Revision Date	Description of Change
December 16, 2021	Preliminary Data Sheet.
May 9, 2022	Changed RF Input Power (Pin Max) from TBD to 23 dBm.
August 25, 2022	Upgraded Evaluation Board Layout from RevB to RevC. Changed C1 to M12 on Evaluation Board BOM and Schematic.
October 3, 2022	Added Thermal Resistance specification.
November 8, 2022	Added characterization plots. Added new S-parameter and Mu plots. Updated evaluation board BOM.
December 22, 2022	Lowered Gain specification from 27.3 to 24.5 dB.
January 27, 2023	Absolute Ratings Table: Added the following condition to Maximum Dissipated Power for Stage 1 & 2: DC only. No RF applied. Changed Stage 1 Maximum Dissipated Power from TBD to 500 mW. Changed Stage 2 Maximum Dissipated Power from TBD to 1400 mW.
February 28, 2023	Added new Characterization Plots. Updated BOM.
June 7, 2023	Release Ø Data Sheet.
September 19, 2023	Release A Data Sheet.
October 12, 2023	Added 2nd and 3rd Harmonics.
July 25, 2024	Upgraded Data Sheet to new format only.
February 14, 2025	Corrected typo on page-7 (condition for Supply Quiescent Current and Supply Current).
May 21, 2025	Updated frequency of family of part numbers listed on page 1.

Data Sheet Classifications

Data Sheet Status	Notes
Advance	S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices.
Preliminary	All data based on evaluation board measurements taken within the Guerrilla RF Applications Lab. Any MIN/MAX limits represented within the data sheet are based solely on *estimated* part-to-part variations and process spreads. All parametric values are subject to change pending the collection of additional data.
Release Ø	All data based on measurements taken with *production-released* material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory.
Release A-Z	All data based on measurements taken with production-released material *derived from multiple lots which have been fabricated over an extended period of time*. MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads.

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