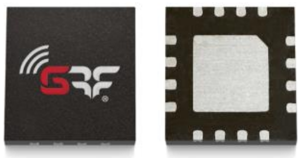
RELEASE Ø DATA SHEET



GRF5606
HIGH LINEARITY POWER AMPLIFIER 663 to 716 MHz

FEATURES

- Excellent OP1dB, OIP3, ACLR and IM3 Performance
- Native Linearity Provides up to +26 dBm P_{OUT} with > 45 dBc ACLR – Without the Need for Digital Predistortion Correction
- +26 dBm Linear Output Power Maintained at 85 °C
- Flexible Biasing Provides Latitude for Linearity Optimization
- 220 mA Native Mode Quiescent Current Consumption
- 5 V Supply Voltage
- 50 Ω Single-ended Input and Output Impedances
- Digital Shutdown
- Rugged Design is Extremely Resilient to Mismatched Loads
- -40 to 85 °C Operating Temperature Range
- Compact 3 x 3 mm QFN-16 Package

Reference: 5 V / 220 mA I_{CCQ} / 698 MHz

- Gain: 27.5 dB
- OIP3: 50 dBm @ +25 dBm P_{OUT}/tone
- OP1dB: 35.6 dBm
- Evaluation Board Noise Figure: 3.9 dB

APPLICATIONS

- Cellular Boosters
- Automotive Compensators
- Picocells/Femtocells
- Customer Premise Equipment

DESCRIPTION

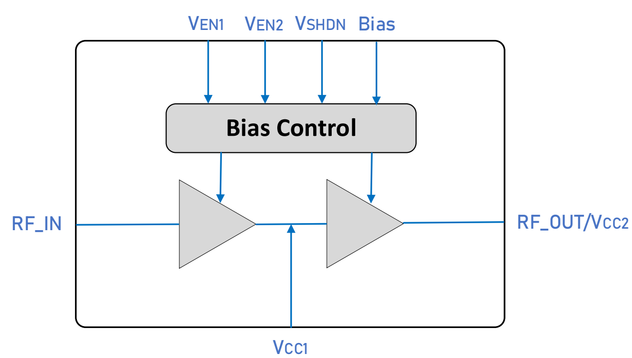
The GRF5606 is a high gain, two-stage InGaP HBT Power Amplifier designed to deliver excellent P1dB, ACLR and IM3 performance over the 663 to 716 MHz band. Its exceptional native linearity makes it an ideal choice for transmitter applications that typically do not employ digital predistortion correction schemes.

This device is part of a complete family of externally matched linear amplifiers that cover the following frequency ranges:

GRF5605: 617 - 652 MHz	GRF5610: 860 - 928 MHz
GRF5606: 663 - 716 MHz	GRF5611: 902 - 960 MHz
GRF5607: 703 - 748 MHz	GRF5616: 1625 - 1675 MHz
GRF5608: 729 - 830 MHz	GRF5617: 1710 - 1785 MHz
GRF5609: 814 - 862 MHz	GRF5618: 1800 - 1920 MHz

Please consult with the GRF applications engineering team for custom tuning/evaluation board data.

BLOCK DIAGRAM



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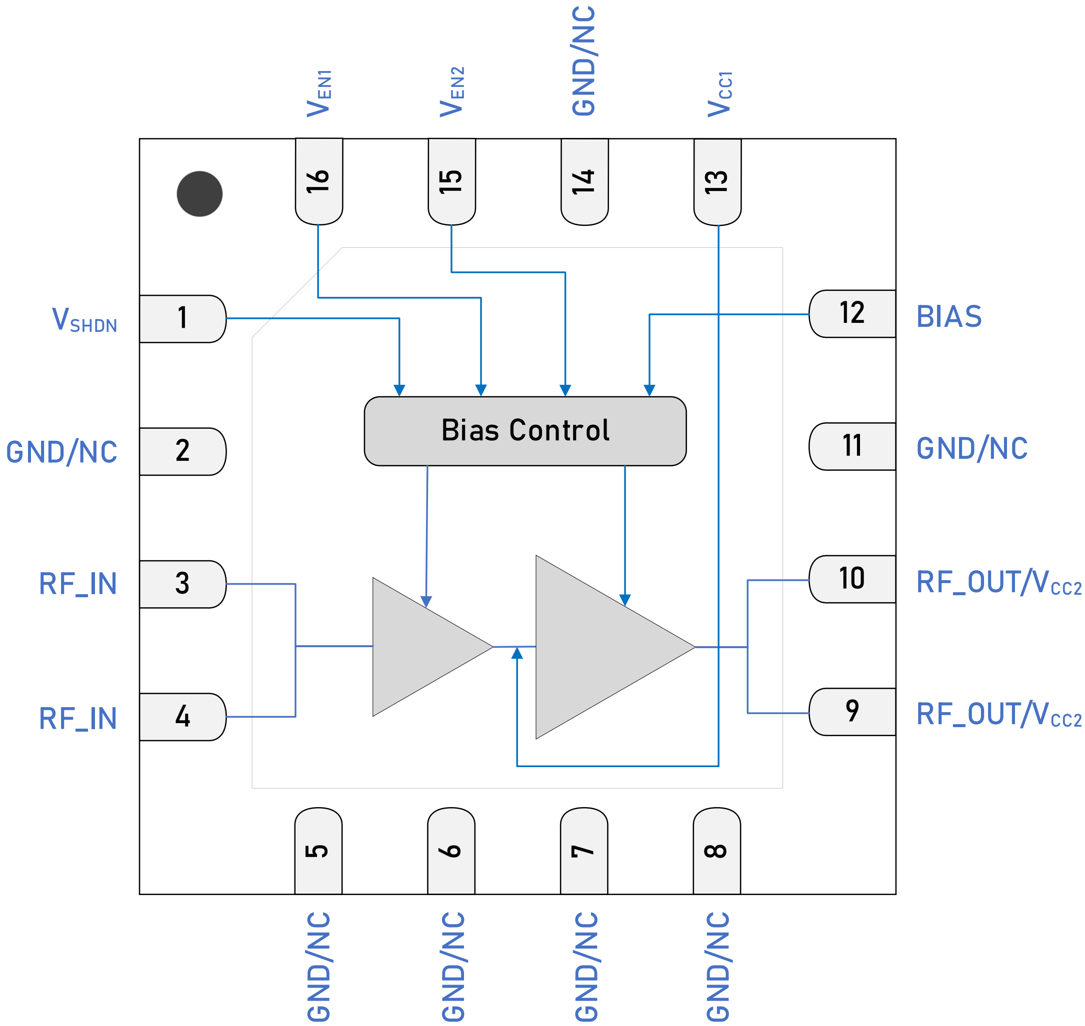

3 x 3 mm QFN-16 Pin Out (Top View)

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Pin Assignments

Pin	Name	Description	Note
1	V_{SHDN}	Digital Shutdown Pin	V_{SHDN} ≥ 1.8 V (Logic HIGH) disables device. V_{SHDN} ≤ 0.8 V (Logic LOW) enables device.
2, 5, 6, 7, 8, 11, 14	GND/NC	Ground or No Connect	No internal connection to die. These pins can be left unconnected, or be connected to ground (recommended). Use a via as close to the pin as possible if grounded.
3, 4	RF_IN	RF Input	Pins 3 & 4 tied together on system board. An external DC blocking cap must be used.
9, 10	RF_OUT/V_{CC2}	PA Output/Bias Voltage	Pins 9 & 10 tied together on system board. V_{CC2} must be applied to this pin via an RF choke.
12	Bias	Bias Circuit Supply	Connect to V_{CC2} through external resistor.
13	V_{CC1}	Bias Voltage	Connect to V_{CC1} through external inductor and capacitive termination (see application schematic).
15	V_{EN2}	Enable2 Voltage Input	V_{EN2} and series resistor set I_{CCQ} for the output stage. V_{EN2} ≤ 0.2 volts disables stage 2.
16	V_{EN1}	Enable1 Voltage Input	V_{EN1} and series resistor set I_{CCQ} for the input stage. V_{EN1} ≤ 0.2 volts disables stage 1. Connecting an external de-coupling capacitor to ground is required for optimal NF performance.
PKG BASE	GND	Ground	Provides DC and RF ground for the amplifier, as well as thermal heat sink. Recommend multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page.

Truth Table

Pin	Logic	Condition
V_{SHDN}	LOW	Full Operation
	HIGH	All Amplifiers Off
V_{EN1}	LOW	Stage 1 Amplifier Off
	HIGH	Stage 1 Amplifier On
V_{EN2}	LOW	Stage 2 Amplifier Off
	HIGH	Stage 2 Amplifier On

Absolute Ratings

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage		V_{CC}	3	5.25	V
RF Input Power	50 Ω, V_{CC} = 5 V, CW Tone, 100% Duty Cycle, $T_{PKG\ BASE}$ = 25 °C	$P_{IN\ MAX-1:1}$		20	dBm
	Load VSWR ≤ 8:1, all phase angles, V_{CC} = 5 V, CW Tone, 100% Duty Cycle, $T_{PKG\ BASE}$ = -40 to 85 °C	$P_{IN\ MAX-8:1}$		7	
Operating Temperature (package base)		$T_{PKG\ BASE}$	-40	85	°C
Maximum Junction Temperature (MTTF >10^6 Hours)		$T_{J\ MAX}$		190	°C
Maximum Dissipated Power Stage 1: DC only (no RF applied).		$P_{DISS\ MAX}$		*500	mW
Maximum Dissipated Power Stage 2: DC only (no RF applied).		$P_{DISS\ MAX}$		*1350	mW
Shutdown Voltage		V_{SHDN}		**5.25	V

Electrostatic Discharge

Human Body Model	HBM	1000		V

Storage

Storage Temperature	T_{STG}	-65	150	°C
Moisture Sensitivity Level	MSL		1	--

* Bias resistors M5/M9 have been empirically optimized for linearity. Thus, there will be no benefit in decreasing resistance (thereby increasing I_{CCQ}).
** M4 = 0 Ω. V_{SHDN} = 5.25 V yields I_{SHDN} = 540 µA. I_{SHDN} decreases linearly vs V_{SHDN} (to 65 µA with V_{SHDN} = 1.8 V).
Said linear relationship can be used to scale M4 for higher V_{SHDN} voltage: use the pin condition V_{SHDN_pin}/I_{SHDN} = 2.4V/147µA.
Calculate M4 for V_{SHDN}/I_{SHDN} = 5V/147µA: M4 = (5–2.4)/(0.000147) = 17.7 kΩ.

Caution! ESD Sensitive Device.
Exceeding Absolute Maximum Rating conditions may cause permanent damage.

Note: For additional information, please refer to *Manufacturing Note MN-001 — Package and Manufacturing Information.*

All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging requiring no exemptions . Additional information for this topic can be found at this link - *Environmental and Restricted Substance Statement Library*

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Recommended Operating Conditions

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	3	5	5.25	V	
Operating Temperature (package base)	$T_{PKG\ BASE}$	-40		85	°C	
RF Frequency Range	F_{RF}	663		716	MHz	Typical application schematic using the 663 to 716 MHz tuning set **(note 1)**.
RF_IN Port Impedance	Z_{RFIN}		50		Ω	Single-ended with 2-element match.
RF_OUT Port Impedance	Z_{RFOUT}		50		Ω	Single-ended with 5-element match.

Note 1: Contact the Guerrilla RF applications team for guidance on optimizing the tuning of the device for alternative bands.

Nominal Operating Parameters – General

The following conditions apply unless noted otherwise: typical application schematic using the 663 to 716 MHz tuning set, V_{CC} = 5 V, V_{SHDN} = LOW, I_{CCQ} = 220 mA, P_{OUT} = +25 dBm, F_{TEST} = 698 MHz, M5 = 2.1 kΩ, M9 = 4.64 kΩ, 50 Ω system impedance, $T_{PKG\ BASE}$ = 25 °C. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Supply Quiescent Current	I_{CCQ}		220		mA	I_{CCQ1} + I_{CCQ2}. No RF applied.
Supply Current with RF Applied	I_{CC}		310		mA	I_{CC1} + I_{CC2}. RF applied with P_{OUT} = +25 dBm.
Enable Current 1	$I_{ENABLE1}$		1.8		mA	V_{CC} = 5 V.
Enable Current 2	$I_{ENABLE2}$		0.5		mA	V_{CC} = 5 V.
Operating Temperature Range	$T_{PKG\ BASE}$	-40		85	°C	Measured on package base.
Logic Input Low	V_{IL}	0		0.8	V	Applies to V_{SHDN} Input.
Logic Input High	V_{IH}	1.8		V_{CC}	V	Applies to V_{SHDN} Input.
Logic Current Low	I_{IL}		1.3		nA	Applies to V_{SHDN} Input, V_{IL} = 0.8 V.
Logic Current High	I_{IH}		65		µA	Applies to V_{SHDN} Input, V_{IH} = 1.8 V.
			285			Applies to V_{SHDN} Input, V_{IH} = 3.3 V.
Switching Rise Time	T_{RISE}		80		ns	Applies to V_{SHDN} Input.
Switching Fall Time	T_{FALL}		30		ns	Applies to V_{SHDN} Input.

Disabled Mode

Supply Quiescent Current	$I_{CCQ-SHDN}$		8		µA	V_{CC} = 5 V, $V_{SHDN}/V_{EN1}/V_{EN2}$ = HIGH.
Enable Current 1	$I_{ENABLE1-SHDN}$		2.2		mA	V_{CC} = 5 V, $V_{SHDN}/V_{EN1}/V_{EN2}$ = HIGH.
Enable Current 2	$I_{ENABLE2-SHDN}$		0.9		mA	V_{CC} = 5 V, $V_{SHDN}/V_{EN1}/V_{EN2}$ = HIGH.

Thermal Data: Stage 1 and Stage 2

Stage 1: Thermal Resistance (Infrared Scan). DC only (no RF applied)	ΘJC		116		°C/W	
Stage 2: Thermal Resistance (Infrared Scan). DC only (no RF applied)	ΘJC		31		°C/W	
See plot of Die Temp vs. Output Power	Tj				°C	On standard evaluation board **(note 2)**.

Note 2: MTTF >10^6 hours for T_J ≤190 °C.

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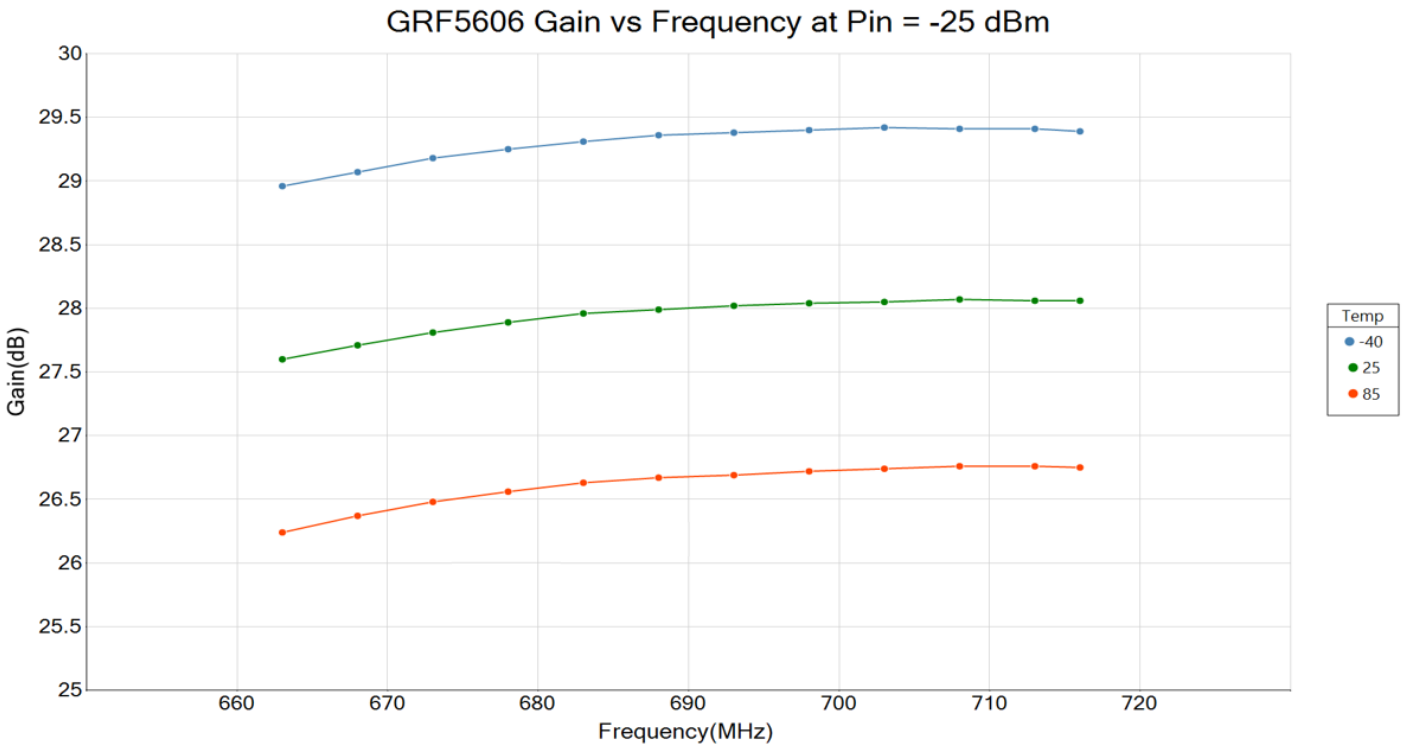
Nominal Operating Parameters – RF: 663 to 716 MHz, 5 V

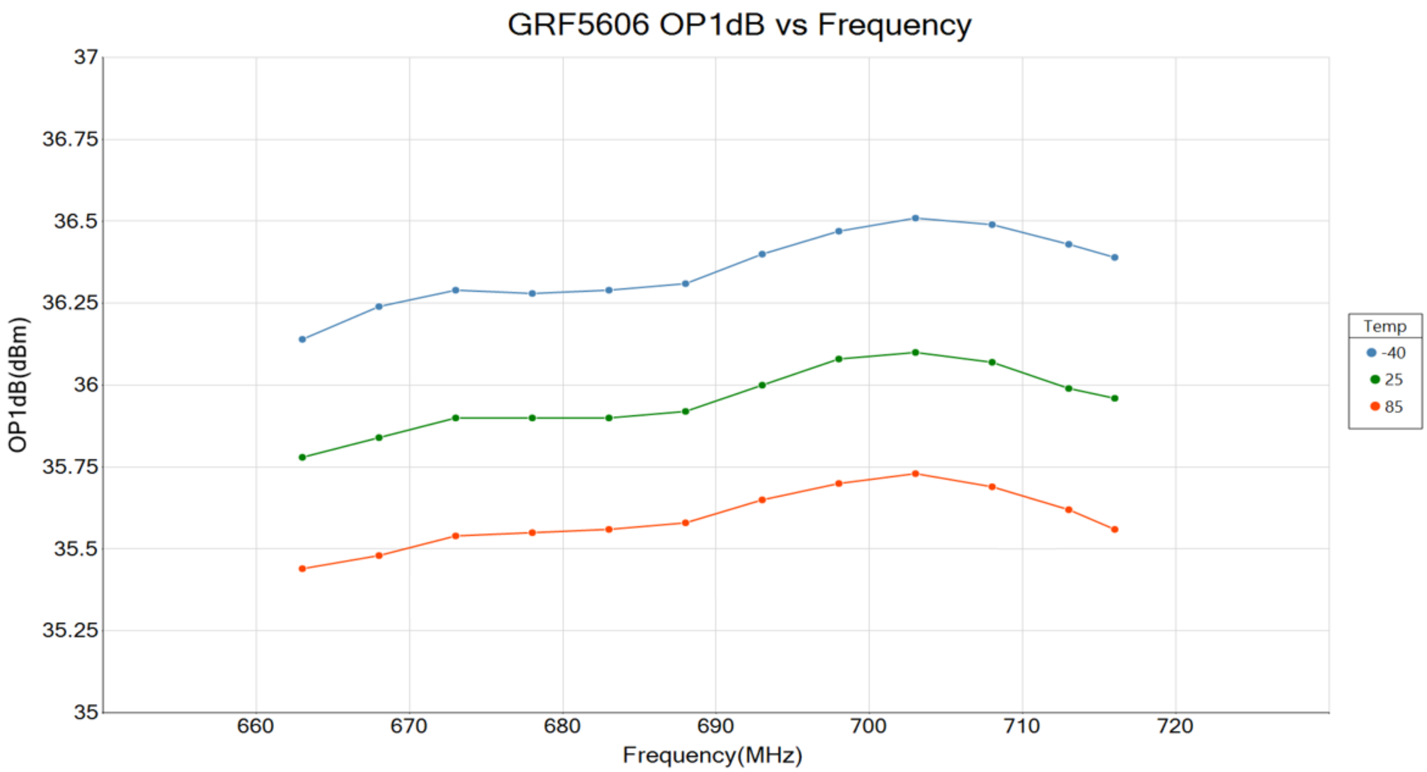
The following conditions apply unless noted otherwise: typical application schematic using the 663 to 716 MHz tuning set, V_{CC} = 5 V, V_{SHDN} = LOW, I_{CCQ} = 220 mA, P_{OUT} = +25 dBm, F_{TEST} = 698 MHz, M5 = 2.1 kΩ, M9 = 4.64 kΩ, 50 Ω system impedance, $T_{PKG\ BASE}$ = 25 °C. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Small Signal Gain	S21		27.5		dB	F_{TEST} = 698 MHz, V_{CC} = 5 V, P_{IN} = -25 dBm.
Standby Mode Gain	$S21_{STBY}$		-39		dB	Disabled mode, $V_{SHDN}/V_{EN1}/V_{EN2}$ = HIGH, P_{IN} = 0 dBm.
Input Return Loss	S11		< -14		dB	F_{RF} = 663 to 716 MHz.
Output Return Loss	S22		< -4.5		dB	F_{RF} = 663 to 716 MHz.
Reverse Isolation	S12		< -53		dB	F_{RF} = 663 to 716 MHz.
Noise Figure	NF		3.9		dB	On standard evaluation board.
Output 3rd Order Intercept Point	OIP3		50		dBm	+25 dBm P_{OUT} per tone at 600 kHz spacing.
Output 1 dB Compression Power	OP1dB		35.6		dBm	V_{CC} = 5 V, Sine wave input.
Adjacent Channel Leakage Ratio	ACLR		-47		dBc	P_{OUT} = +25 dBm, LTE 20MHz 100RB TM1.1 Downlink Waveform with 9.6dB PAR, F_{TEST} = 698 MHz, V_{CC} = 5 V **(note 3)**.

Note 3: MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. As additional production lots are fabricated, accumulated test data will be used to refine the MIN/MAX limits.

GRF5606 Typical Operating Curves:





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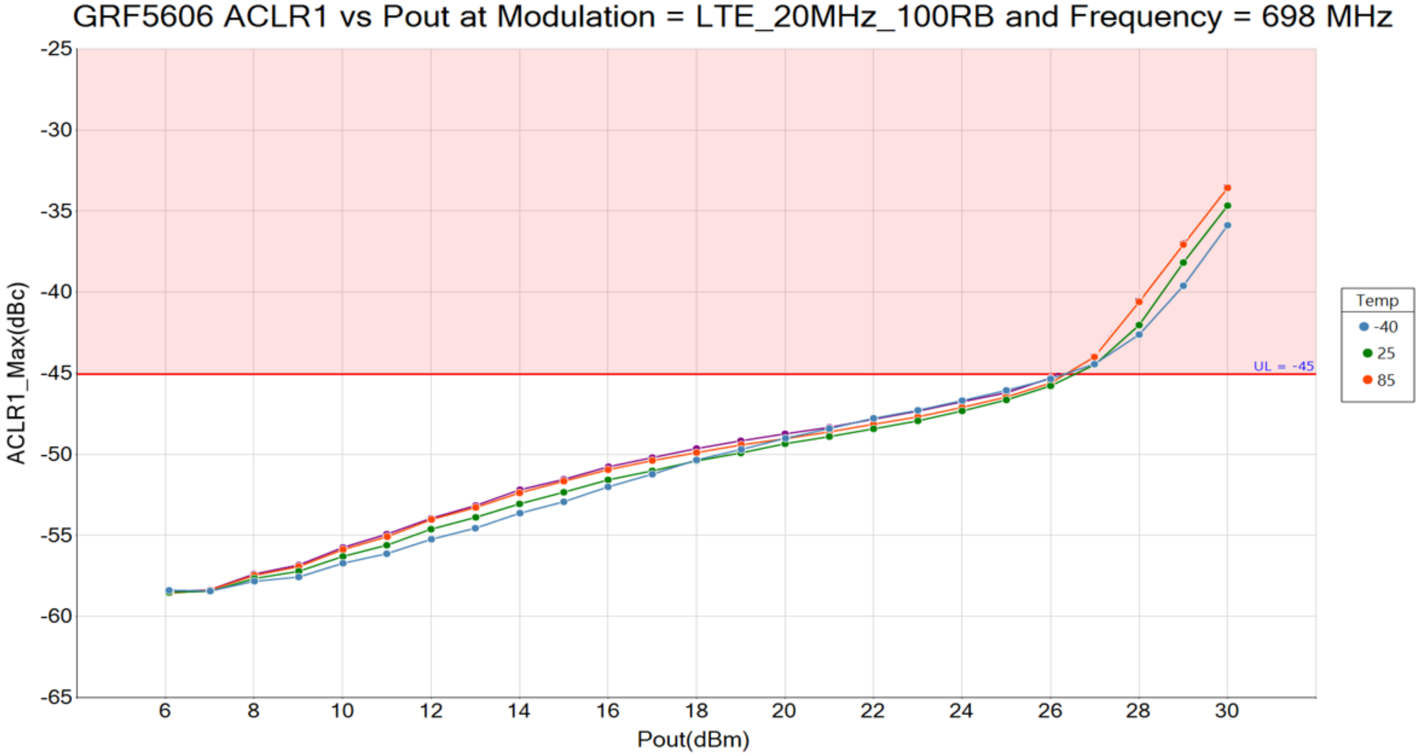
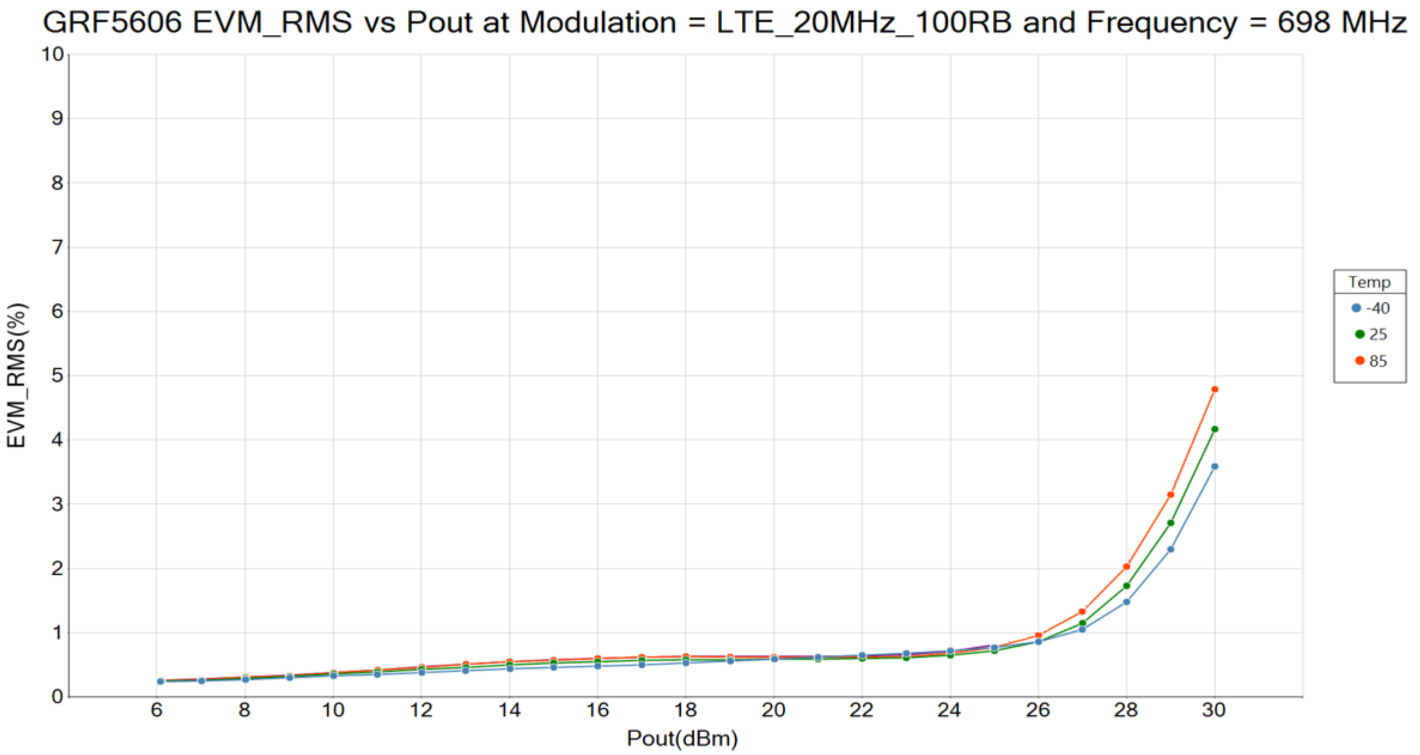
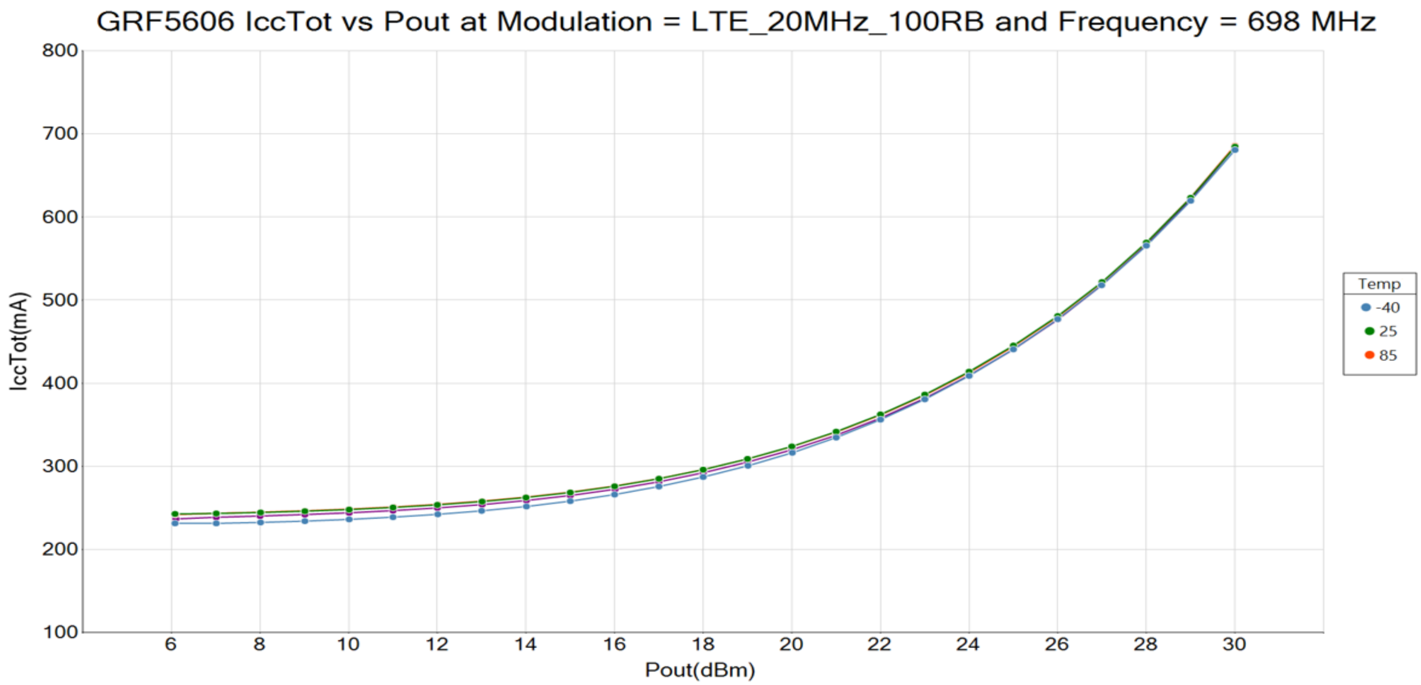
GRF5606 Typical Operating Curves:





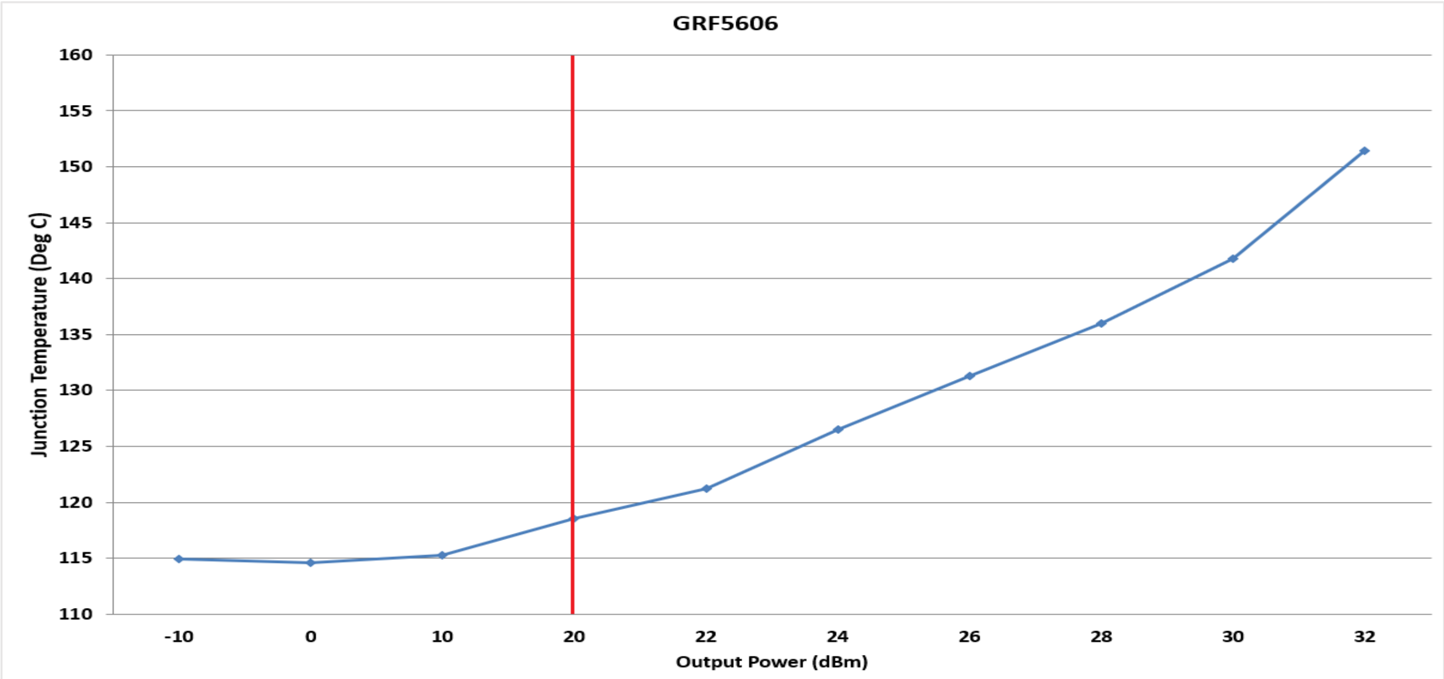
GRF5606 Typical Operating Curves:



Junction Temperature: per application schematic @ 85 °C

GRF5606, being a 2-stage device, sees one of the stages governing junction temperature over power sweep. Red line = 20 dBm shows where T_J is equivalent in both stages. At left of red line, stage 1 governs T_J (Q1 T_J is higher). To the right of red line, stage 2 governs T_J (Q2 T_J is higher).

Setting bias resistor M5/M9 per application schematic ensures best linearity and yields thermal performance shown in the plot. If the application does not require high IMD3/ACLR linearity, bias resistors can be adjusted higher. This will lower bias point(s) and junction temperature will be contained within/below that shown in the plot.



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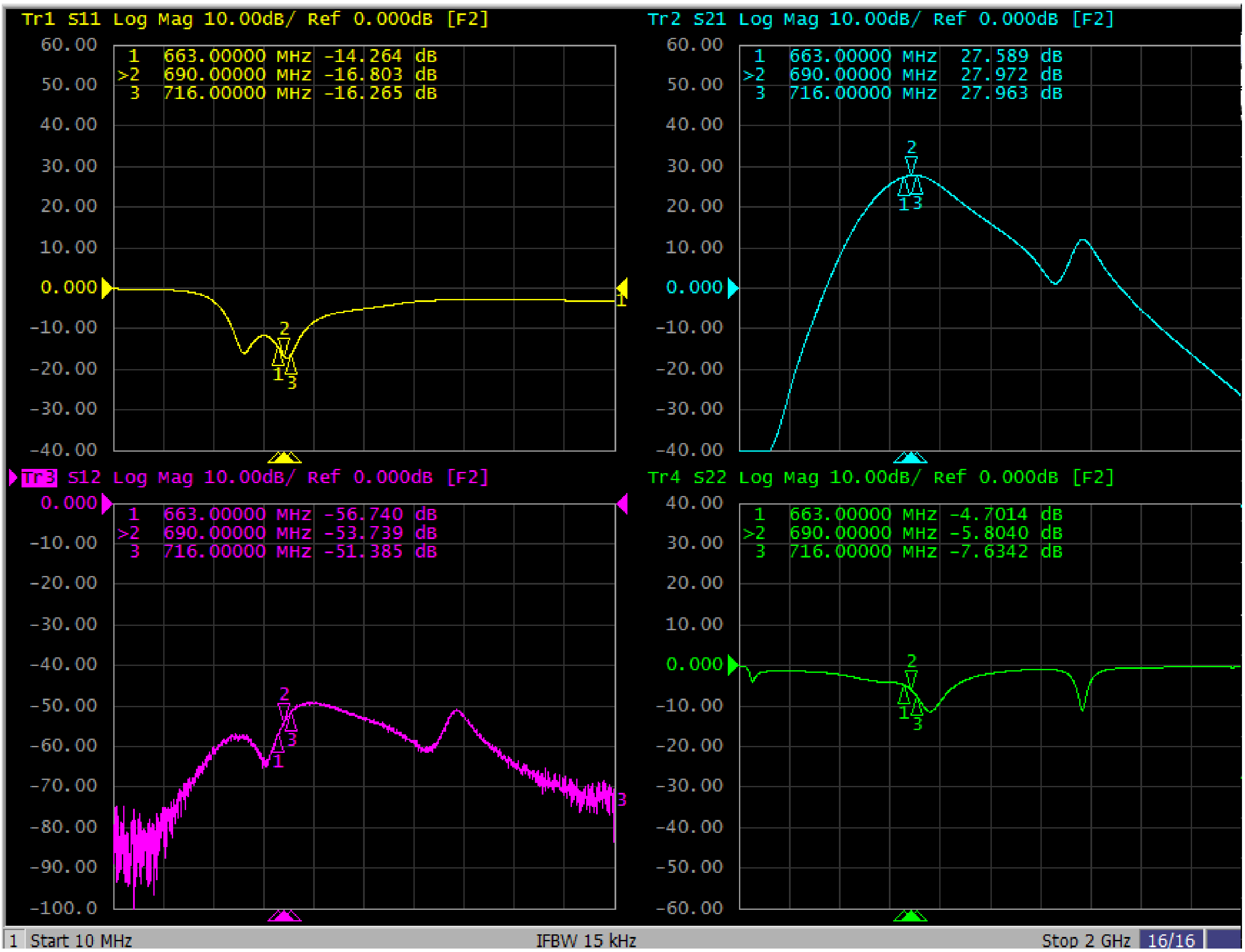
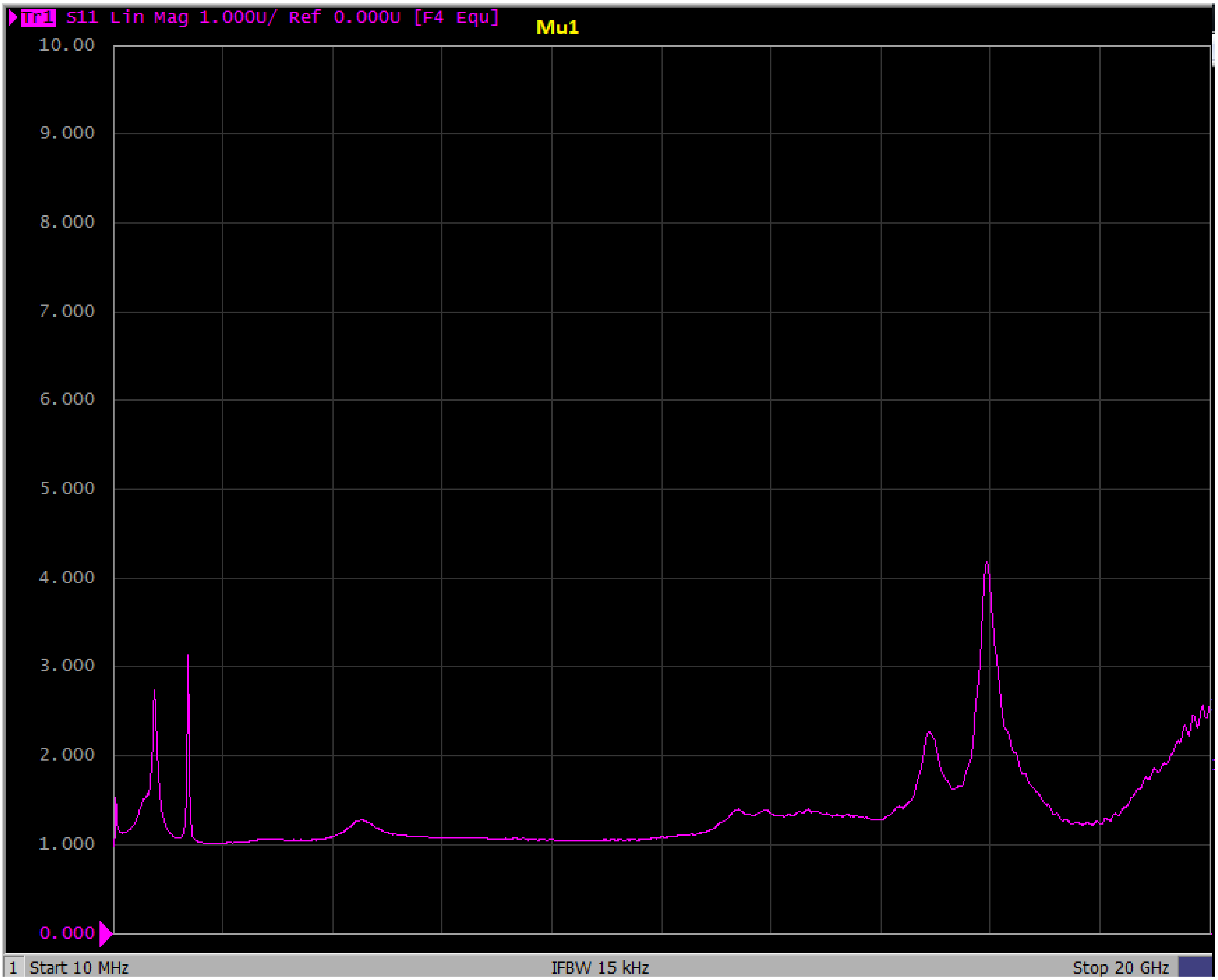
GRF5606 Typical Operating Curves: S-Parameters (663 to 716 MHz Tune)



GRF5606 Typical Operating Curves: Stability Mu (10 MHz to 20 GHz)



Note: Mu factor ≥ 1.0 implies unconditional stability.

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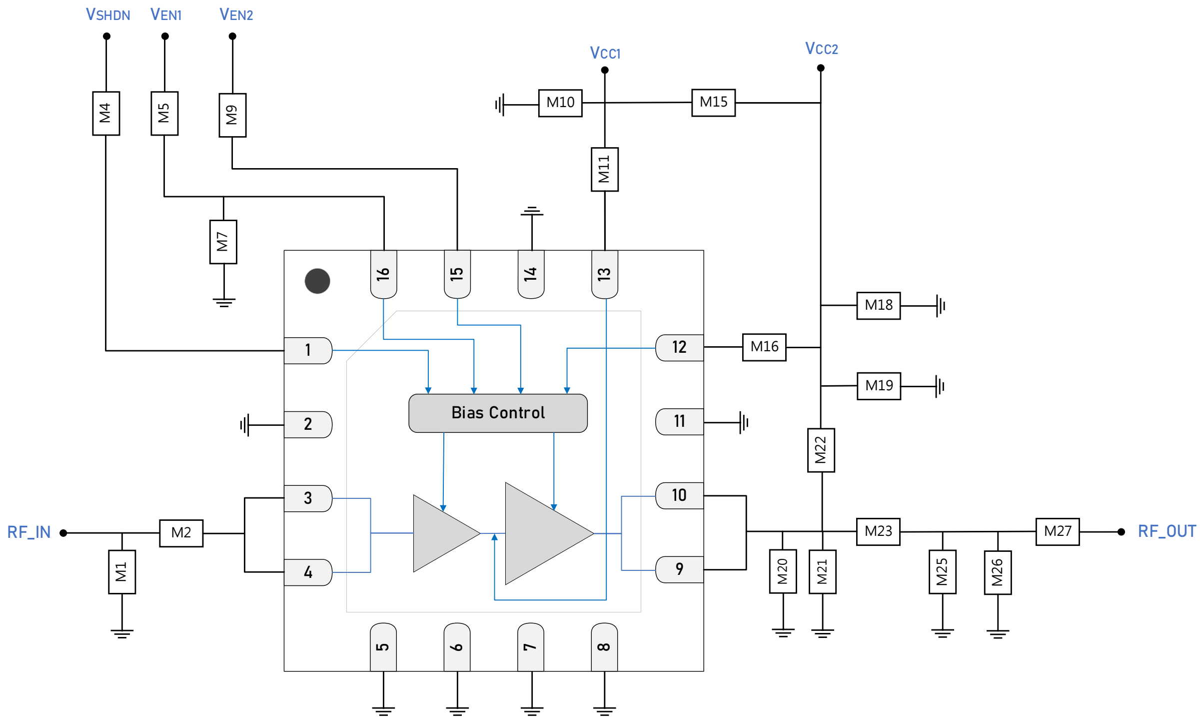
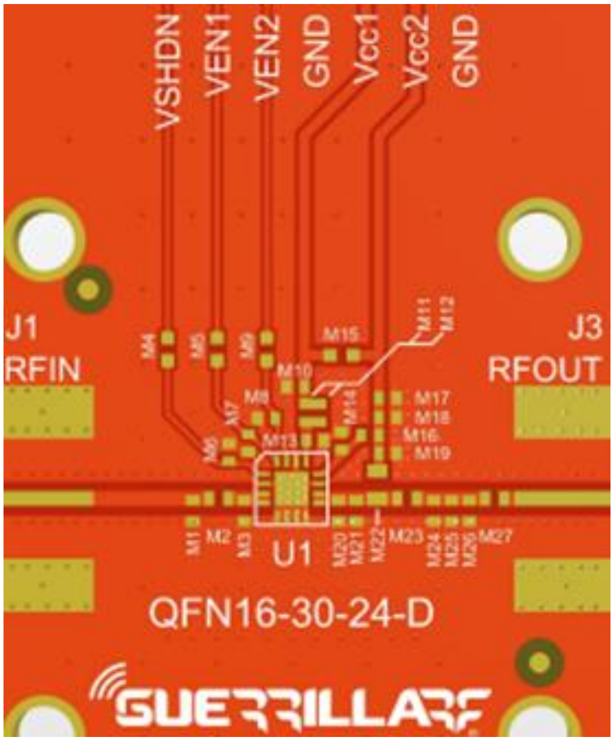


GRF5606 Standard Evaluation Board Schematic



GRF5606 Evaluation Board Assembly Diagram

GRF5606 Evaluation Board Assembly Diagram Reference

Component	Type	Manufacturer	Family	Value	Package Size	Substitution
M1	Inductor	Murata	LQG	7.5 nH	0402	ok
M2	Capacitor	Murata	GJM	12 pF	0402	ok
M4	Resistor	Various	--	0 Ω	0402	ok
M5	Resistor	Various	1%	2100 Ω	0402	ok
M7	Capacitor	Murata	GRM	100 pF	0402	ok
M9	Resistor	Various	1%	4640 Ω	0402	ok
M10	Capacitor	Murata	GRM	0.1 µF	0402	ok
M11	Inductor	Coilcraft	0402HP	12 nH	0402	ok
M15	Resistor	Various	--	0 Ω	0402	ok
M16	Resistor	Various	--	0 Ω	0402	ok
M18	Capacitor	Murata	**GRM	10 µF	0402	ok
M19	Capacitor	Murata	GRM	100 pF	0402	ok
M20	Capacitor	Murata	GJM	3.6 pF	0402	ok
M21	Capacitor	Murata	GJM	12 pF	0404	ok
M22	Inductor	Coilcraft	0807SQ	14 nH	0807	ok
M23	Inductor	Coilcraft	0402DC	1.2 nH	0402	ok
M25	Capacitor	Murata	GJM	9.1 pF	0402	ok
M26	Capacitor	Murata	GJM	1.8 pF	0402	ok
M27	Capacitor	Murata	GRM	100 pF	0402	ok
Evaluation Board	QFN16-30-24-D					

Note: Standard evaluation board bias: V_{CC} = 5 V, V_{ENABLE} = 5 V.

** 10 µF must be rated for > 5 V at maximum ambient temperature. Manufacturer Part Number in this case = GRM155C80J106ME11D.

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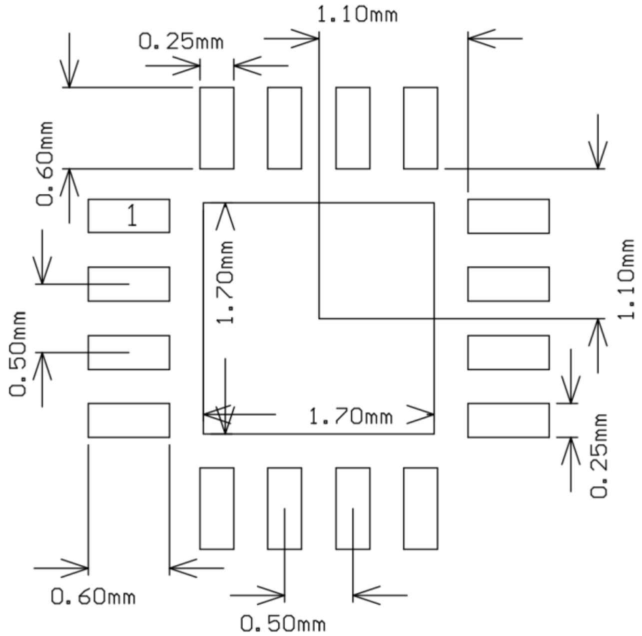
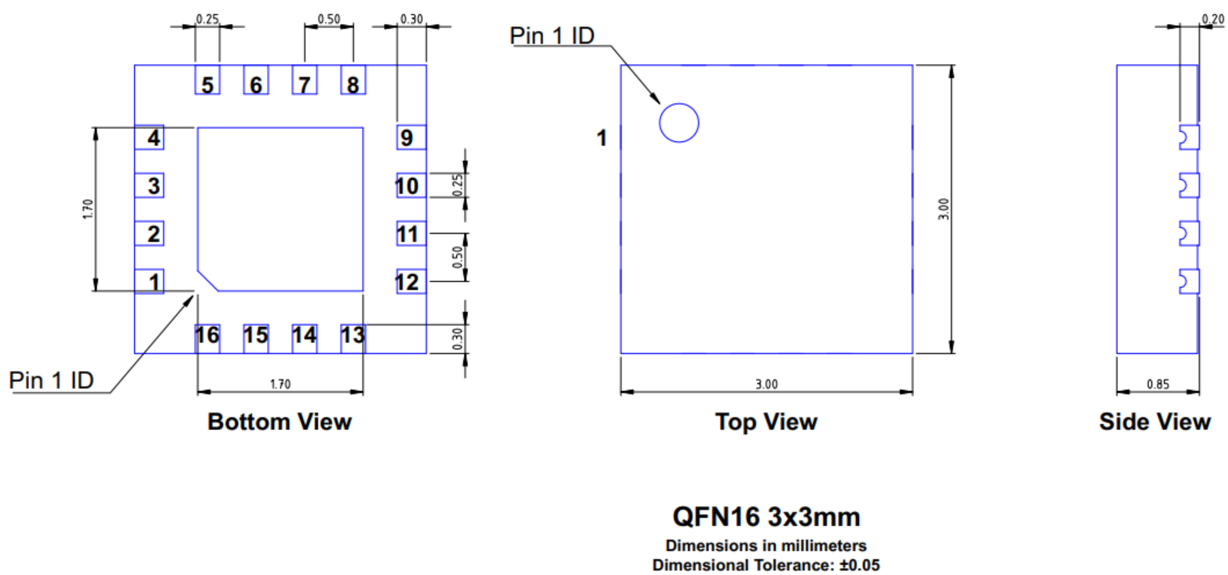


3 x 3 mm QFN-16 Suggested PCB Footprint (Top View)



3 x 3 mm QFN-16 Package Dimensions

Package Marking Diagram

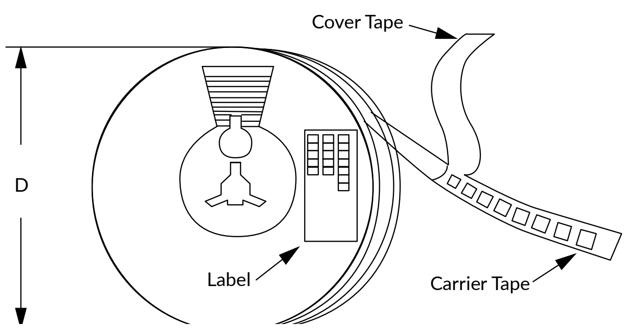
- Line 1: "YY" = YEAR. "WW" = WORK WEEK the device was assembled.
- Line 2: "GRF" = Guerrilla RF.
- Line 3: "XXXX" = Device PART NUMBER.

Tape and Reel Information

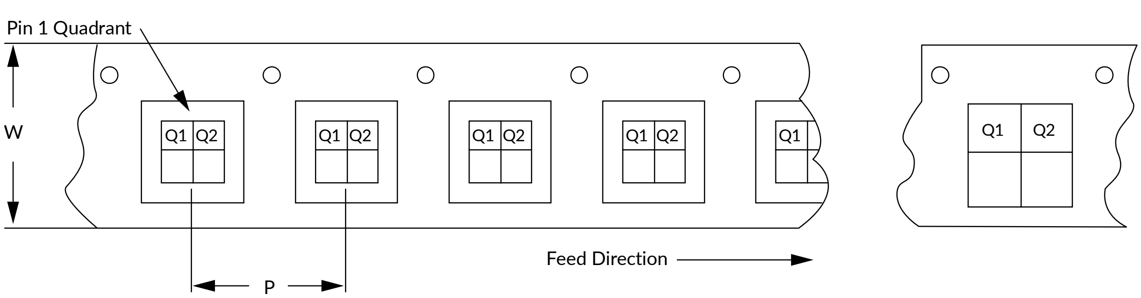
Guerrilla RF's tape and reel specification complies with Electronic Industries Alliance (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). See the following page for the Tape and Reel Specification and Device Package Information table, which includes units per reel.

Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag and the outside surface of the box.

For the Tape and Reel Reference Table, please refer to: *https://www.guerrilla-rf.com/prodFiles/Manufacturing/MN001.pdf*



Tape and Reel Packaging with Reel Diameter Noted (D)



Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information

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Revision History

Revision Date	Description of Change
September 28, 2021	Preliminary Data Sheet.
March 8, 2022	Updated Package Marking Diagram.
February 14, 2024	Release Ø Data Sheet. Updated Evaluation Board to RevD.
January 20, 2025	Updated Data Sheet with minor cosmetic changes only. No change to device or device specifications.
June 11, 2025	Page 1: updated lower frequency range for GRF5608 and GRF5610.

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Data Sheet Classifications

Data Sheet Status	Notes
Advance	S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices.
Preliminary	All data based on limited evaluation board measurements taken within the Guerrilla RF Applications Lab. All parametric values are subject to change pending the collection of additional data.
Release Ø	All data based on measurements taken with *production-released* material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory.
Release A-Z	All data based on measurements taken with production-released material *derived from multiple lots which have been fabricated over an extended period of time.* MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads.