

## GRF5607

### HIGH LINEARITY POWER AMPLIFIER 703 to 748 MHz

#### FEATURES

- Excellent OP1dB, OIP3, ACLR and IM3 Performance
- Native Linearity Provides up to +26 dBm  $P_{OUT}$  with > 45 dBc ACLR – Without the Need for Digital Predistortion Correction
- +26 dBm Linear Output Power Maintained at 85 °C
- Flexible Biasing Provides Latitude for Linearity Optimization
- 227 mA Native Mode Quiescent Current Consumption
- 5 V Supply Voltage
- 50  $\Omega$  Single-ended Input and Output Impedances
- Digital Shutdown
- Rugged Design is Extremely Resilient to Mismatched Loads
- -40 to 85 °C Operating Temperature Range
- Compact 3 x 3 mm QFN-16 Package

#### Reference: 5 V / 227 mA $I_{CCQ}$ / 725 MHz

- Gain: 29 dB
- OIP3: 49 dBm @ 25 dBm  $P_{OUT}/tone$
- OP1dB: 34.9 dBm
- Evaluation Board Noise Figure: 4.1 dB

#### APPLICATIONS

- Cellular Boosters
- Automotive Compensators
- Picocells/Femtocells
- Customer Premise Equipment

#### DESCRIPTION

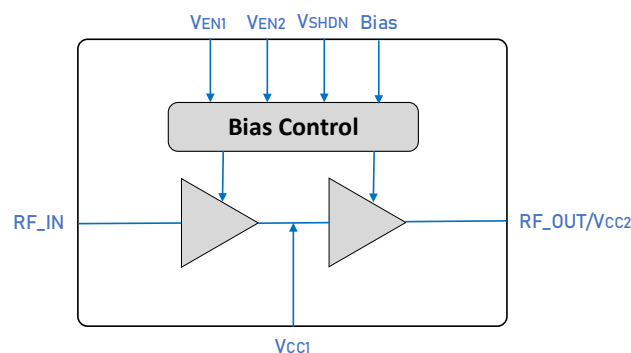
The GRF5607 is a high gain, two-stage InGaP HBT Power Amplifier designed to deliver excellent P1dB, ACLR and IM3 performance over the 703 to 748 MHz band. Its exceptional native linearity makes it an ideal choice for transmitter applications that typically do not employ digital predistortion correction schemes.

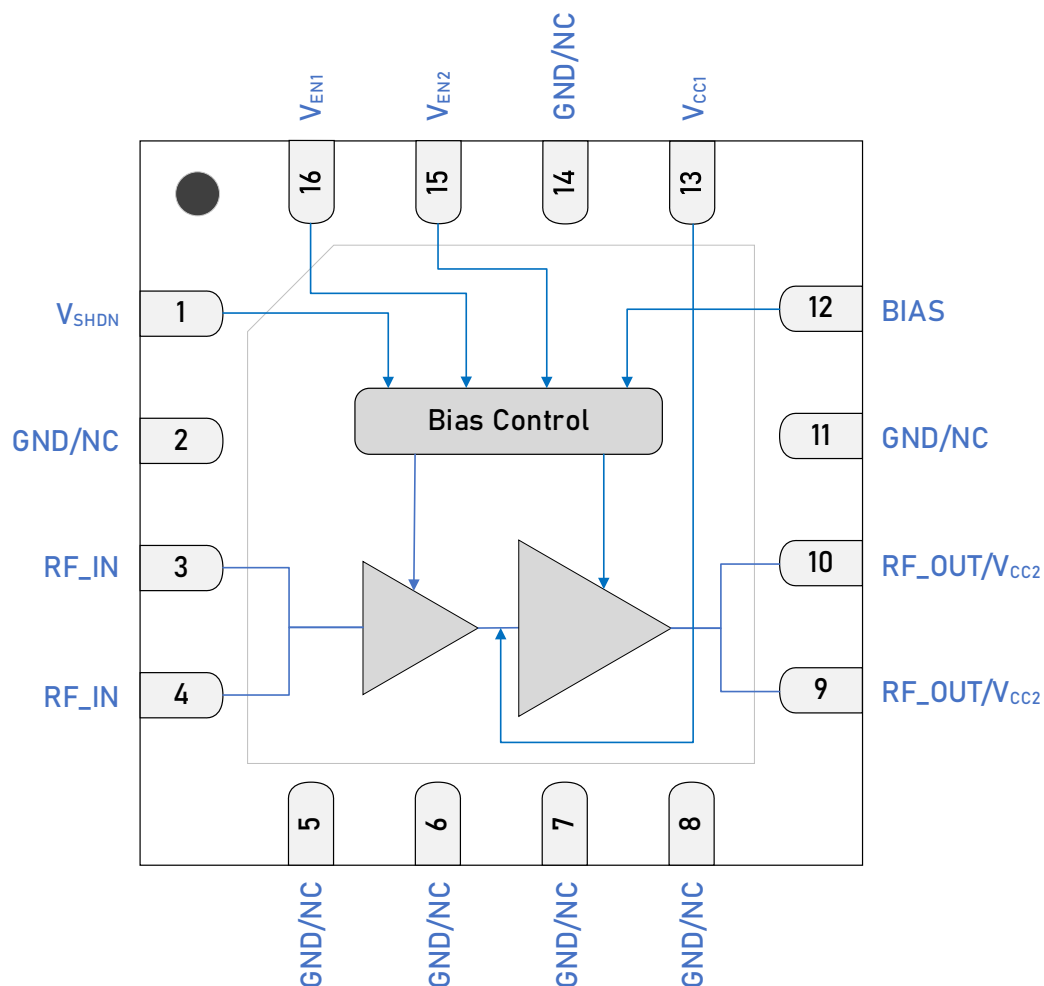
This device is part of a complete family of externally matched linear amplifiers that cover the following frequency ranges:

|                        |                          |
|------------------------|--------------------------|
| GRF5605: 617 - 652 MHz | GRF5610: 860 - 928 MHz   |
| GRF5606: 663 - 716 MHz | GRF5611: 902 - 960 MHz   |
| GRF5607: 703 - 748 MHz | GRF5616: 1625 - 1675 MHz |
| GRF5608: 729 - 830 MHz | GRF5617: 1710 - 1785 MHz |
| GRF5609: 814 - 862 MHz | GRF5618: 1800 - 1920 MHz |

Please consult with the GRF applications engineering team for custom tuning/evaluation board data.

#### BLOCK DIAGRAM





3 x 3 mm QFN-16 Pin Out (Top View)

## Pin Assignments

| Pin                   | Name                    | Description            | Note                                                                                                                                                                                                                                |
|-----------------------|-------------------------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                     | V <sub>SHDN</sub>       | Digital Shutdown Pin   | V <sub>SHDN</sub> ≥ 1.8 V (Logic HIGH) disables device. V <sub>SHDN</sub> ≤ 0.8 V (Logic LOW) enables device.                                                                                                                       |
| 2, 5, 6, 7, 8, 11, 14 | GND/NC                  | Ground or No Connect   | No internal connection to die. These pins can be left unconnected, or be connected to ground (recommended). Use a via as close to the pin as possible if grounded.                                                                  |
| 3, 4                  | RF_IN                   | RF Input               | Pins 3 and 4 tied together on system board. An external DC blocking capacitor must be used.                                                                                                                                         |
| 9, 10                 | RF_OUT/V <sub>CC2</sub> | PA Output/Bias Voltage | Pins 9 and 10 tied together on system board. V <sub>CC2</sub> must be applied to this pin via an RF choke.                                                                                                                          |
| f12                   | Bias                    | Bias Circuit Supply    | Connect to V <sub>CC2</sub> through external resistor.                                                                                                                                                                              |
| 13                    | V <sub>CC1</sub>        | Bias Voltage           | Connect to V <sub>CC1</sub> through external inductor and capacitive termination (see application schematic).                                                                                                                       |
| 15                    | V <sub>EN2</sub>        | Enable2 Voltage Input  | V <sub>EN2</sub> and series resistor set I <sub>CCQ</sub> for the output stage. V <sub>EN2</sub> ≤ 0.2 volts disables stage 2.                                                                                                      |
| 16                    | V <sub>EN1</sub>        | Enable1 Voltage Input  | V <sub>EN1</sub> and series resistor set I <sub>CCQ</sub> for the input stage. V <sub>EN1</sub> ≤ 0.2 volts disables stage 1. Connecting an external decoupling capacitor to ground is required for optimal NF performance.         |
| PKG BASE              | GND                     | Ground                 | Provides DC and RF ground for the amplifier, as well as thermal heat sink. Recommend multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page. |

## Truth Table

| Pin               | Logic | Condition             |
|-------------------|-------|-----------------------|
| V <sub>SHDN</sub> | LOW   | Full Operation        |
|                   | HIGH  | All Amplifiers Off    |
| V <sub>EN1</sub>  | LOW   | Stage 1 Amplifier Off |
|                   | HIGH  | Stage 1 Amplifier On  |
| V <sub>EN2</sub>  | LOW   | Stage 2 Amplifier Off |
|                   | HIGH  | Stage 2 Amplifier On  |

## Absolute Ratings

| Parameter                                                    |                                                                                                                    | Symbol              | Min. | Max.    | Unit |
|--------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|---------------------|------|---------|------|
| Supply Voltage                                               |                                                                                                                    | $V_{CC}$            | 3    | 5.25    | V    |
| RF Input Power                                               | 50 $\Omega$ , $V_{CC} = 5$ V, CW Tone, 100% Duty Cycle, $T_{PKG\ BASE} = 25$ °C.                                   | $P_{IN\ MAX - 1:1}$ |      | 20      | dBm  |
|                                                              | Load VSWR $\leq 8:1$ , all phase angles, $V_{CC} = 5$ V, CW Tone, 100% Duty Cycle, $T_{PKG\ BASE} = -40$ to 85 °C. | $P_{IN\ MAX - 8:1}$ |      | 15      |      |
| Operating Temperature (package base).                        |                                                                                                                    | $T_{PKG\ BASE}$     | -40  | 85      | °C   |
| Maximum Junction Temperature (MTTF > 10 <sup>6</sup> Hours). |                                                                                                                    | $T_{J\ MAX}$        |      | 190     | °C   |
| Maximum Dissipated Power Stage 1: DC only (no RF applied).   |                                                                                                                    | $P_{DISS\ MAX}$     |      | * 450   | mW   |
| Maximum Dissipated Power Stage 2: DC only (no RF applied).   |                                                                                                                    | $P_{DISS\ MAX}$     |      | * 1350  | mW   |
| Shutdown Voltage                                             |                                                                                                                    | $V_{SHDN}$          |      | ** 5.25 | V    |

## Electrostatic Discharge

|                  |     |      |  |   |
|------------------|-----|------|--|---|
| Human Body Model | HBM | 1000 |  | V |
|------------------|-----|------|--|---|

## Storage

|                            |           |     |     |    |
|----------------------------|-----------|-----|-----|----|
| Storage Temperature        | $T_{STG}$ | -65 | 150 | °C |
| Moisture Sensitivity Level | MSL       |     | 1   | -- |

\* Bias resistors M5/M9 have been empirically optimized for linearity. Thus, there will be no benefit in decreasing resistance (thereby increasing  $I_{CCQ}$ ).

\*\* M4 = 0  $\Omega$ .  $V_{SHDN} = 5.25$  V yields  $I_{SHDN} = 540$   $\mu$ A.  $I_{SHDN}$  decreases linearly vs  $V_{SHDN}$  (to 65  $\mu$ A with  $V_{SHDN} = 1.8$  V).

Said linear relationship can be used to scale M4 for higher  $V_{SHDN}$  voltage: use the pin condition  $V_{SHDN\_pin}/I_{SHDN} = 2.4V/147\mu A$ .

Calculate M4 for  $V_{SHDN}/I_{SHDN} = 5V/147\mu A$ :  $M4 = (5-2.4)/(0.000147) = 17.7$  k $\Omega$ .



**Caution! ESD Sensitive Device.**

**Exceeding Absolute Maximum Rating conditions may cause permanent damage.**

Note: For additional information, please refer to [Manufacturing Note MN-001 — Package and Manufacturing Information](#).



All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging requiring no exemptions. Additional information for this topic can be found at this link - [Environmental and Restricted Substance Statement Library](#)

## Recommended Operating Conditions

| Parameter                            | Symbol          | Specification |      |      | Unit     | Condition                                                                                     |
|--------------------------------------|-----------------|---------------|------|------|----------|-----------------------------------------------------------------------------------------------|
|                                      |                 | Min.          | Typ. | Max. |          |                                                                                               |
| Supply Voltage                       | $V_{CC}$        | 3             | 5    | 5.25 | V        |                                                                                               |
| Operating Temperature (package base) | $T_{PKG\ BASE}$ | -40           |      | 85   | °C       |                                                                                               |
| RF Frequency Range                   | $F_{RF}$        | 703           | 725  | 748  | MHz      | Typical application schematic using the 703 to 748 MHz Tuning set ( <b>notes 1 &amp; 2</b> ). |
| RF_IN Port Impedance                 | $Z_{RFIN}$      |               | 50   |      | $\Omega$ | Single-ended with 2-element match.                                                            |
| RF_OUT Port Impedance                | $Z_{RFOUT}$     |               | 50   |      | $\Omega$ | Single-ended with 5-element match.                                                            |

**Note 1:** Operation outside this range is possible but with degraded performance of some parameters.

**Note 2:** Contact the Guerrilla RF applications team for guidance on optimizing the tuning of the device for alternative bands.

## Nominal Operating Parameters – General

The following conditions apply unless noted otherwise: typical application schematic using the 703 to 748 MHz tuning set.  $V_{CC} = 5\text{ V}$ ,  $V_{SHDN} = \text{LOW}$ ,  $I_{CCQ} = 227\text{ mA}$ ,  $P_{OUT} = +25\text{ dBm}$ ,  $F_{TEST} = 725\text{ MHz}$ ,  $M5 = 2.5\text{ k}\Omega$ ,  $M9 = 4.55\text{ k}\Omega$ ,  $50\text{ }\Omega$  system impedance,  $T_{PKG\text{ BASE}} = 25\text{ }^{\circ}\text{C}$ . Evaluation board losses are included within the specifications.

| Parameter                      | Symbol                | Specification |      |          | Unit               | Condition                                                          |
|--------------------------------|-----------------------|---------------|------|----------|--------------------|--------------------------------------------------------------------|
|                                |                       | Min.          | Typ. | Max.     |                    |                                                                    |
| Supply Quiescent Current       | $I_{CCQ}$             |               | 227  |          | mA                 | $I_{CCQ1} + I_{CCQ2}$ . No RF applied.                             |
| Supply Current with RF Applied | $I_{CC}$              |               | 393  |          | mA                 | $I_{CC1} + I_{CC2}$ . RF Applied with $P_{OUT} = +25\text{ dBm}$ . |
| Enable Current 1               | $I_{ENABLE1}$         |               | 1.9  |          | mA                 | $V_{CC} = 5\text{ V}$ .                                            |
| Enable Current 2               | $I_{ENABLE2}$         |               | 0.9  |          | mA                 | $V_{CC} = 5\text{ V}$ .                                            |
| Operating Temperature Range    | $T_{PKG\text{ BASE}}$ | -40           |      | 85       | $^{\circ}\text{C}$ | Measured on package base.                                          |
| Logic Input Low                | $V_{IL}$              | 0             |      | 0.8      | V                  | Applies to $V_{SHDN}$ Input.                                       |
| Logic Input High               | $V_{IH}$              | 1.8           |      | $V_{CC}$ | V                  | Applies to $V_{SHDN}$ Input.                                       |
| Logic Current Low              | $I_{IL}$              |               | 1.3  |          | nA                 | Applies to $V_{SHDN}$ Input, $V_{IL} = 0.8\text{ V}$ .             |
| Logic Current High             | $I_{IH}$              |               | 65   |          | $\mu\text{A}$      | Applies to $V_{SHDN}$ Input, $V_{IH} = 1.8\text{ V}$ .             |
|                                |                       |               | 285  |          |                    | Applies to $V_{SHDN}$ Input, $V_{IH} = 3.3\text{ V}$ .             |
| Switching Rise Time            | $T_{RISE}$            |               | 100  |          | ns                 | Applies to $V_{SHDN}$ Input.                                       |
| Switching Fall Time            | $T_{FALL}$            |               | 20   |          | ns                 | Applies to $V_{SHDN}$ Input.                                       |

### Disabled Mode

|                          |                           |  |     |  |               |                                                                    |
|--------------------------|---------------------------|--|-----|--|---------------|--------------------------------------------------------------------|
| Supply Quiescent Current | $I_{CCQ\text{-SHDN}}$     |  | 15  |  | $\mu\text{A}$ | $V_{CC} = 5\text{ V}$ , $V_{SHDN}/V_{EN1}/V_{EN2} = \text{HIGH}$ . |
| Enable Current 1         | $I_{ENABLE1\text{-SHDN}}$ |  | 2.4 |  | mA            | $V_{CC} = 5\text{ V}$ , $V_{SHDN}/V_{EN1}/V_{EN2} = \text{HIGH}$ . |
| Enable Current 2         | $I_{ENABLE2\text{-SHDN}}$ |  | 0.9 |  | mA            | $V_{CC} = 5\text{ V}$ , $V_{SHDN}/V_{EN1}/V_{EN2} = \text{HIGH}$ . |

### Thermal Data (Stage 1 and Stage 2)

|                                                                       |               |  |     |  |                             |                                                                                             |
|-----------------------------------------------------------------------|---------------|--|-----|--|-----------------------------|---------------------------------------------------------------------------------------------|
| Stage 1: Thermal Resistance (Infrared Scan). DC only (no RF applied). | $\Theta_{JC}$ |  | 136 |  | $^{\circ}\text{C}/\text{W}$ | On standard evaluation board.                                                               |
| Stage 2: Thermal Resistance (Infrared Scan). DC only (no RF applied). | $\Theta_{JC}$ |  | 31  |  | $^{\circ}\text{C}/\text{W}$ | On standard evaluation board.                                                               |
| Thermal Data Stage 1 & 2: See plot of junction Temp vs. Output Power. | $T_J$         |  |     |  | $^{\circ}\text{C}$          | $V_{CC} = V_{EN1} = V_{EN2} = 5\text{ V}$ . On standard evaluation board ( <b>note 3</b> ). |

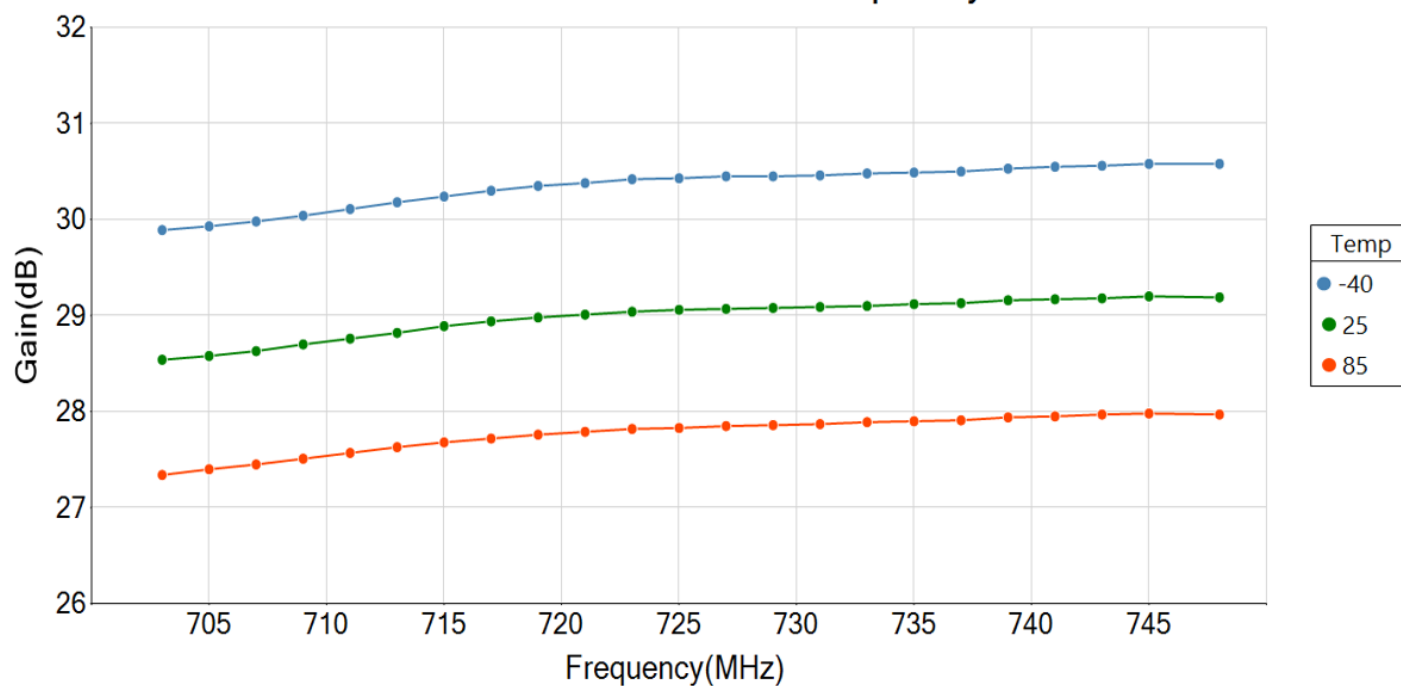
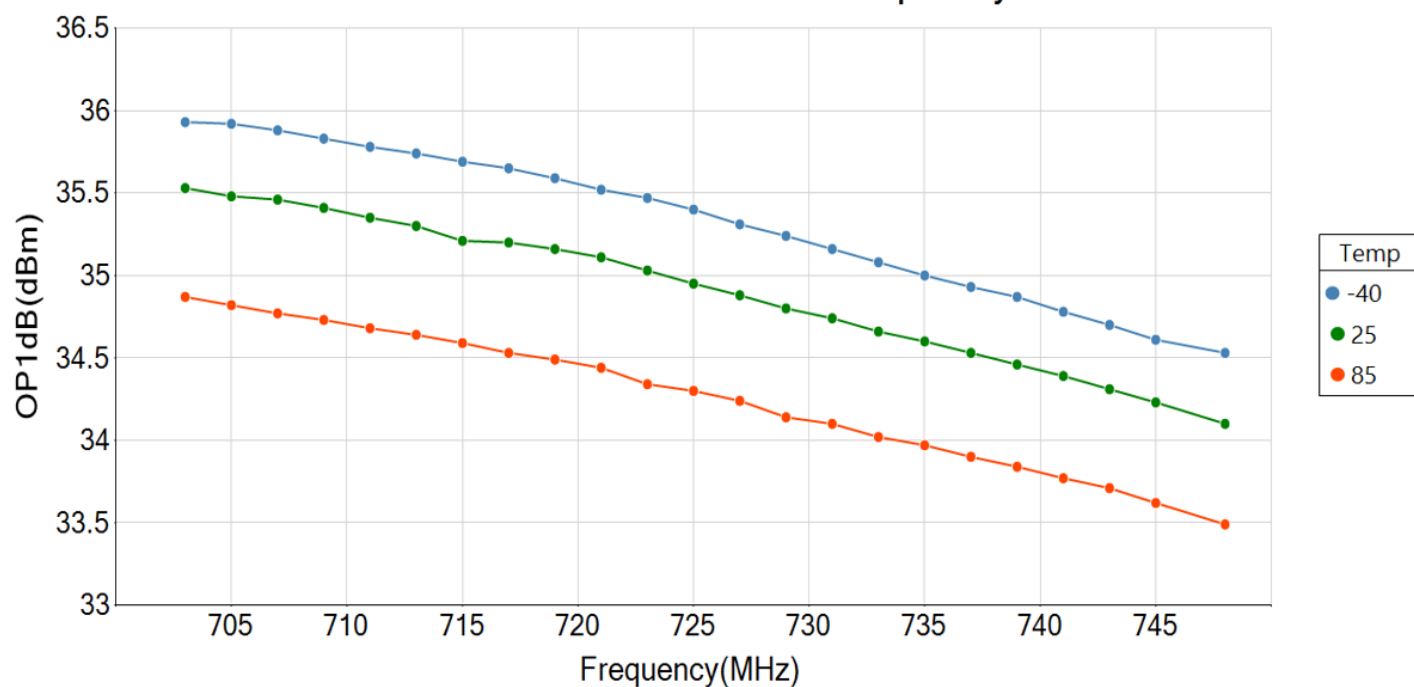
**Note 3:** MTTF >  $10^6$  hours for  $T_J \leq 190\text{ }^{\circ}\text{C}$ .

## Nominal Operating Parameters – RF: 703 to 748 MHz, 5 V Operation

The following conditions apply unless noted otherwise: typical application schematic using the 703 to 748 MHz tuning set.  $V_{CC} = 5\text{ V}$ ,  $V_{SHDN} = \text{LOW}$ ,  $I_{CCQ} = 227\text{ mA}$ ,  $P_{OUT} = +25\text{ dBm}$ ,  $F_{TEST} = 725\text{ MHz}$ ,  $M5 = 2.5\text{ k}\Omega$ ,  $M9 = 4.55\text{ k}\Omega$ ,  $50\text{ }\Omega$  system impedance,  $T_{PKG\text{ BASE}} = 25\text{ }^{\circ}\text{C}$ . Evaluation board losses are included within the specifications.

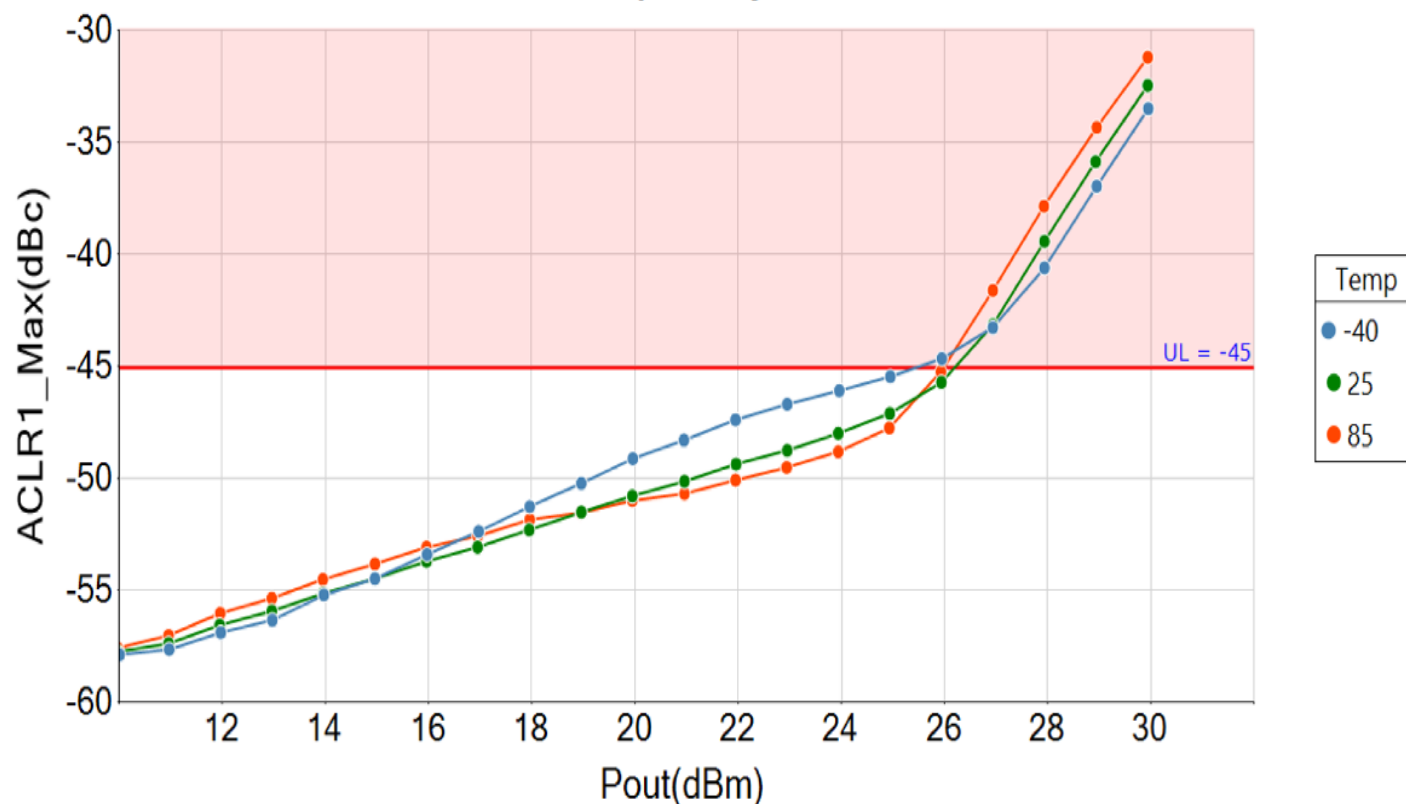
| Parameter                        | Symbol              | Specification |         |      | Unit | Condition                                                                                                                                                  |
|----------------------------------|---------------------|---------------|---------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                  |                     | Min.          | Typ.    | Max. |      |                                                                                                                                                            |
| Small Signal Gain                | S21                 |               | 29      |      | dB   | $F_{TEST} = 725\text{ MHz}$ , $V_{CC} = 5\text{ V}$ , $P_{IN} = -25\text{ dBm}$ .                                                                          |
| Standby Mode Gain                | S21 <sub>STBY</sub> |               | -40     |      | dB   | Disabled mode, $V_{SHDN}/V_{EN1}/V_{EN2} = \text{HIGH}$ , $P_{IN} = 0\text{ dBm}$ .                                                                        |
| Input Return Loss                | S11                 |               | < -13.5 |      | dB   | $F_{RF} = 703\text{ to }748\text{ MHz}$                                                                                                                    |
| Output Return Loss               | S22                 |               | < -6    |      | dB   | $F_{RF} = 703\text{ to }748\text{ MHz}$                                                                                                                    |
| Reverse Isolation                | S12                 |               | < -45   |      | dB   | $F_{RF} = 703\text{ to }748\text{ MHz}$                                                                                                                    |
| Noise Figure                     | NF                  |               | 4.1     |      | dB   | On standard evaluation board.                                                                                                                              |
| Output 3rd Order Intercept Point | OIP3                |               | 49      |      | dBm  | 25 dBm $P_{OUT}$ per tone at 600 kHz spacing.                                                                                                              |
| Output 1 dB Compression Power    | OP1dB               |               | 35      |      | dBm  | Sine wave input, $V_{CC} = 5\text{ V}$ .                                                                                                                   |
| Adjacent Channel Leakage Ratio   | ACLR                |               | -47     |      | dBc  | $P_{OUT} = +25\text{ dBm}$ , LTE 10MHz 50RB TM1.1 Downlink Waveform with 9.6dB PAR, $F_{TEST} = 725\text{ MHz}$ , $V_{CC} = 5\text{ V}$ ( <b>note 4</b> ). |

**Note 4:** MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. As additional production lots are fabricated, accumulated test data will be used to refine the MIN/MAX limits.

**GRF5607 Typical Operating Curves: 703 to 748 MHz Tune**
**GRF5607 Gain vs Frequency**

**GRF5607 OP1dB vs Frequency**


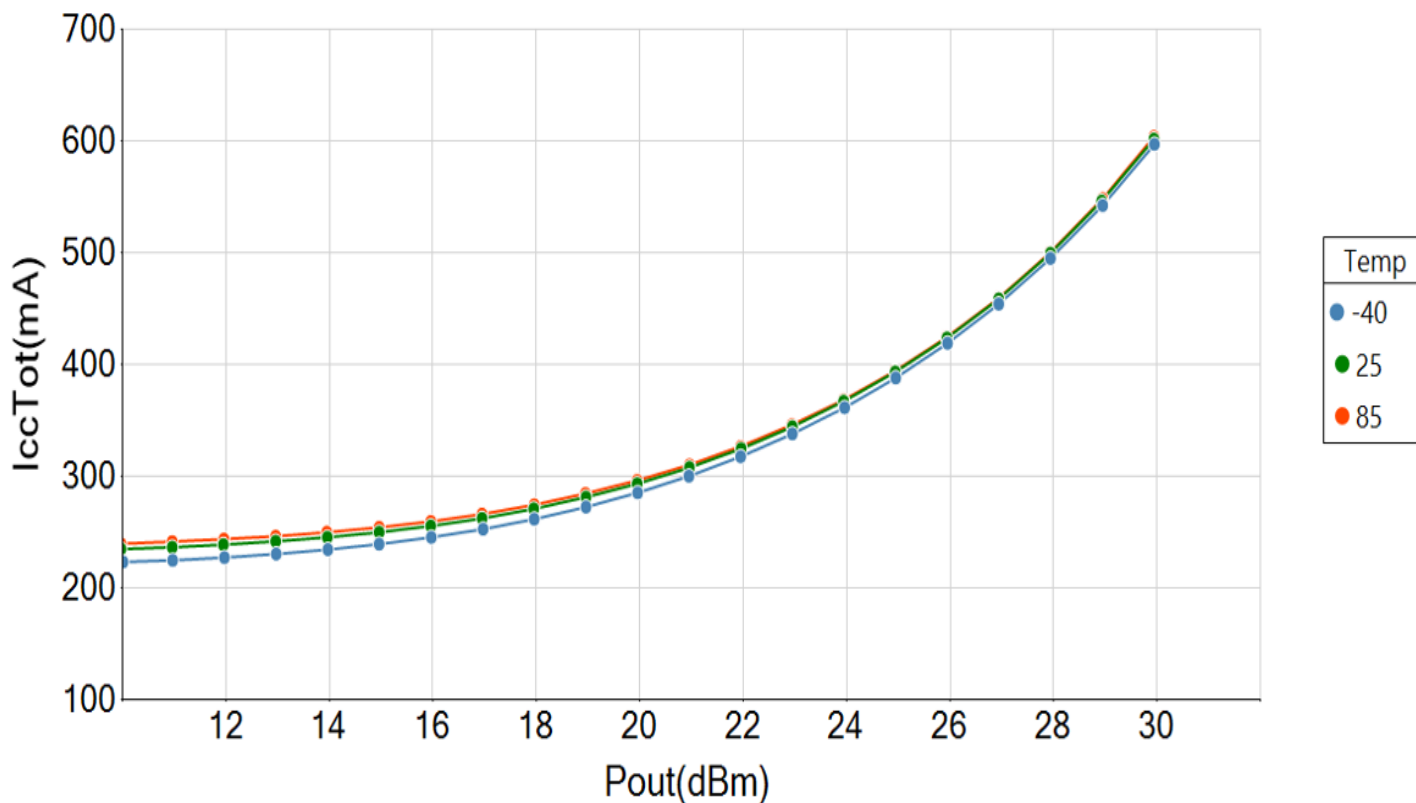
**GRF5607 Typical Operating Curves: ACLR vs. P<sub>OUT</sub> (LTE 20Q100RB TM1.1 9.6 dB PAR)**

**GRF5607 ACLR1 vs Pout at Modulation = LTE\_20MHz\_100RB  
and Frequency = 725 MHz**



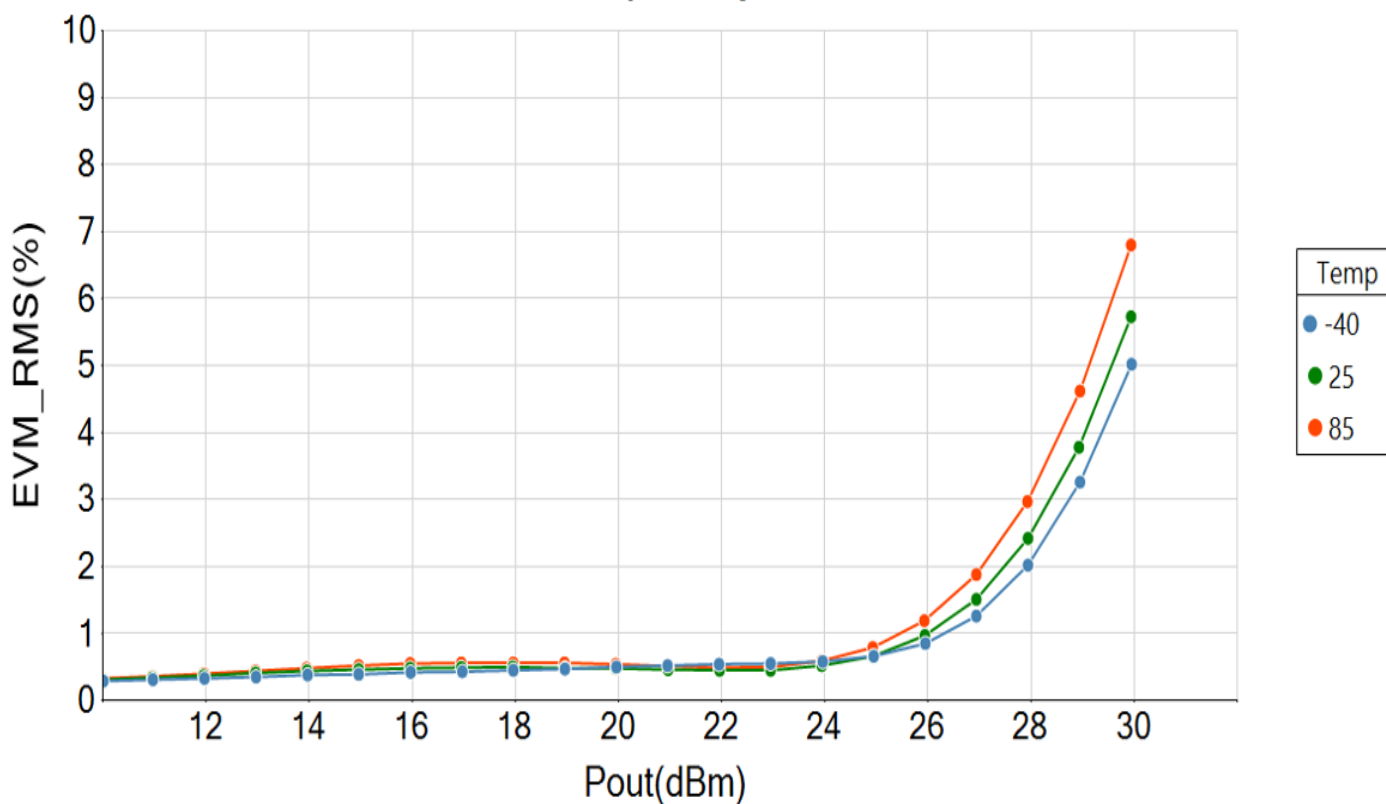
**GRF5607 Typical Operating Curves: Stage1 + Stage2 Icc vs. P<sub>OUT</sub> (LTE 20Q100RB TM1.1 9.6 dB PAR)**

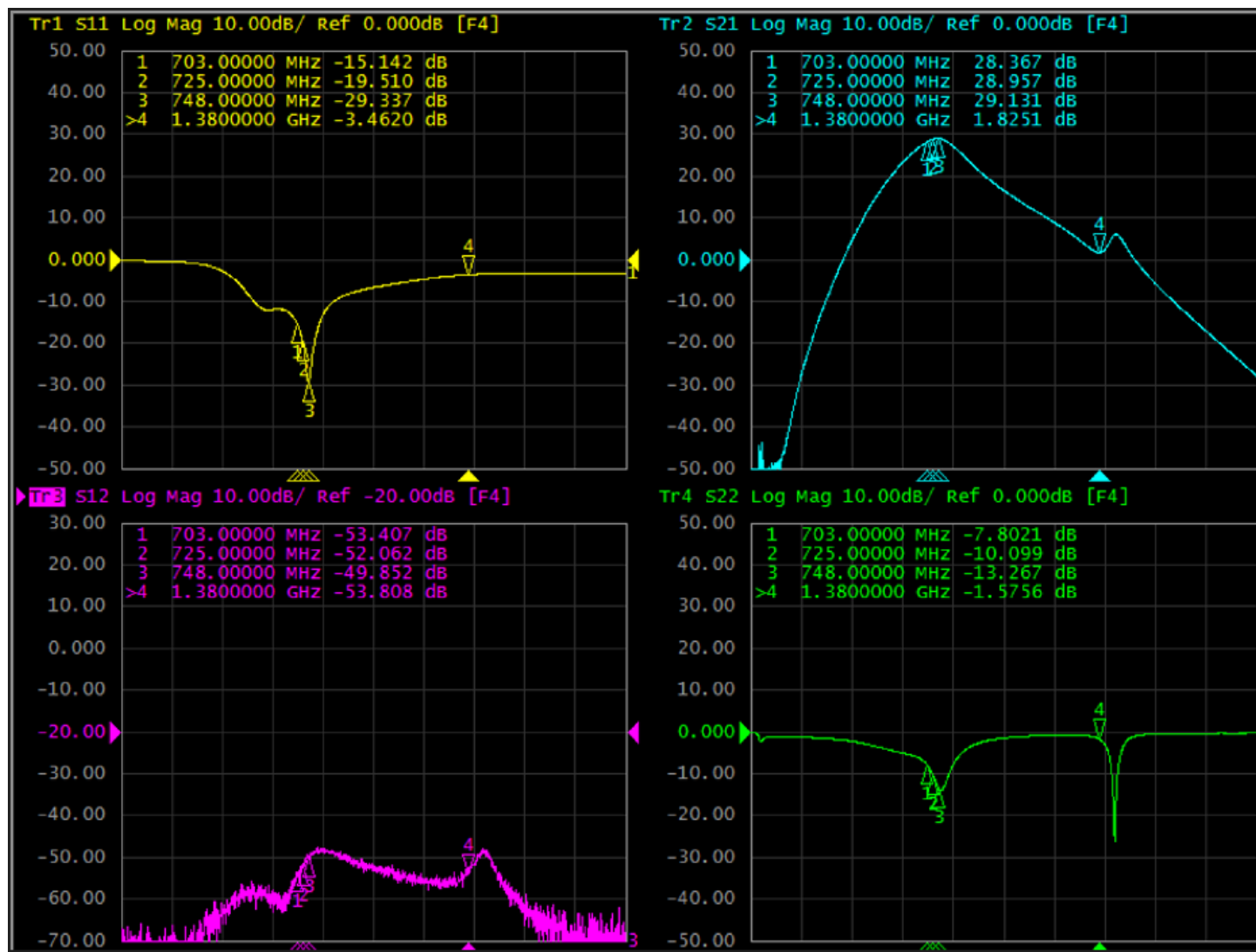
GRF5607 IccTot vs Pout at Modulation = LTE\_20MHz\_100RB and Frequency = 725 MHz



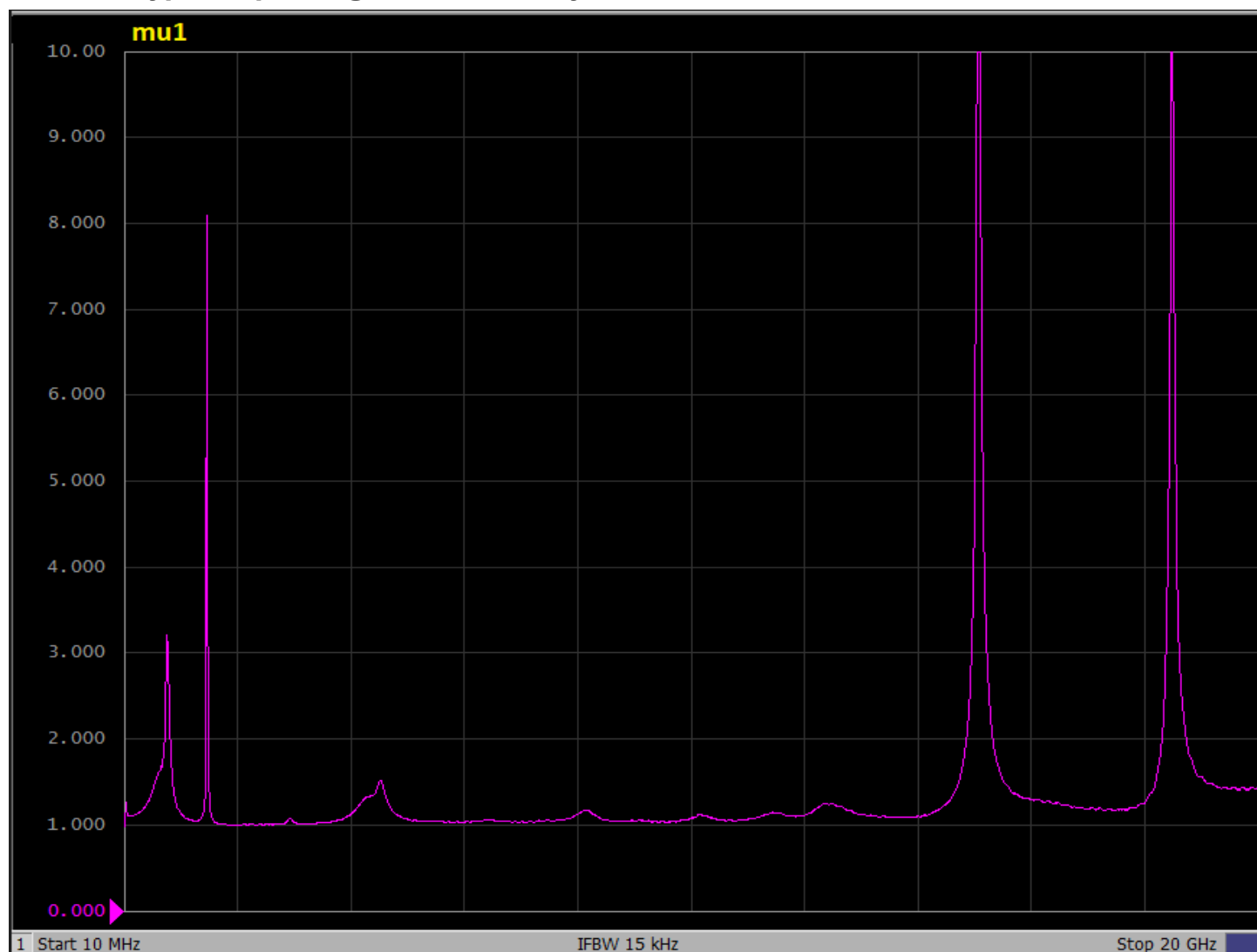
**GRF5607 Typical Operating Curves: 703 to 748 MHz Tune**

**GRF5607 EVM\_RMS vs Pout at Modulation = LTE\_20MHz\_100RB  
and Frequency = 725 MHz**



**GRF5607 Typical Operating Curves: S-Parameters (703 to 748 MHz Tune)**


### GRF5607 Typical Operating Curves: Stability Mu (10 MHz to 20 GHz)

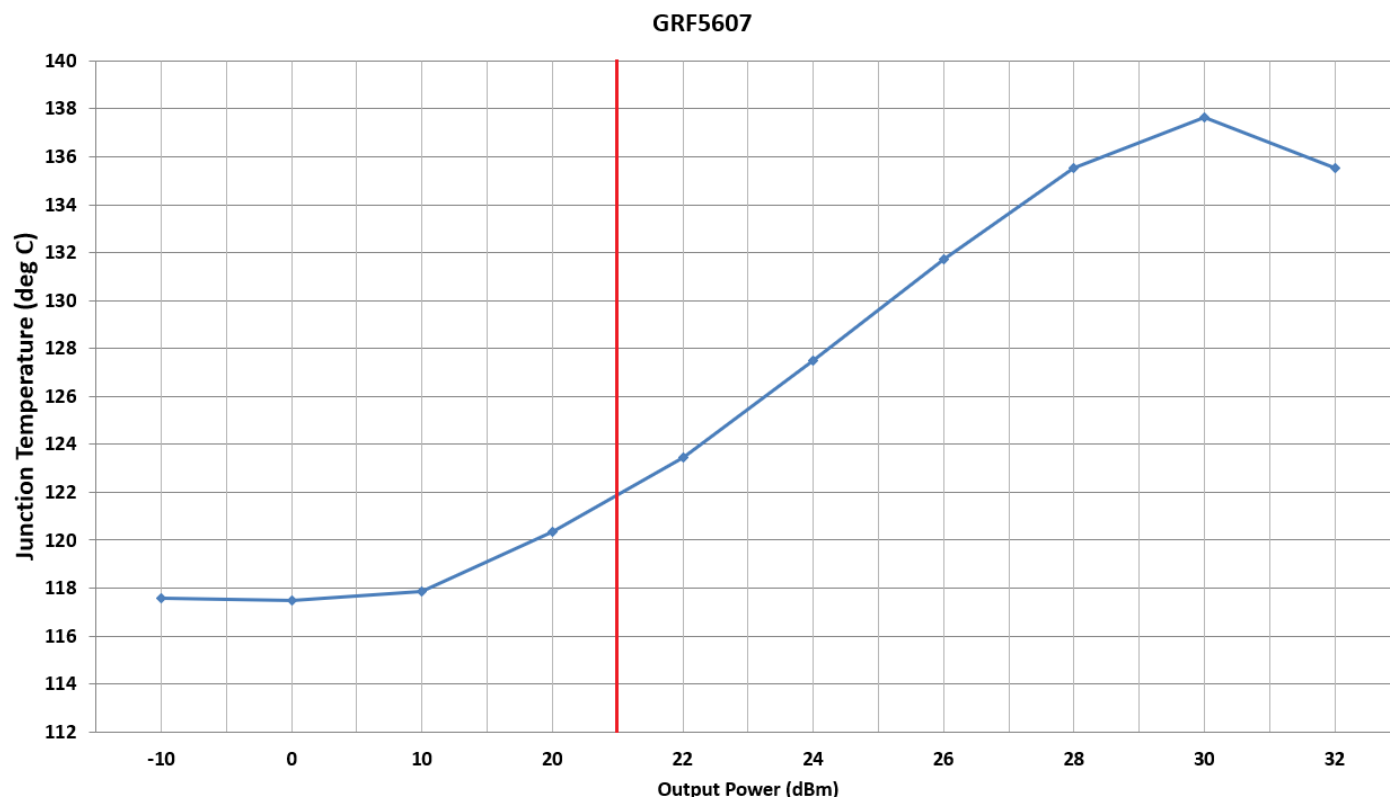


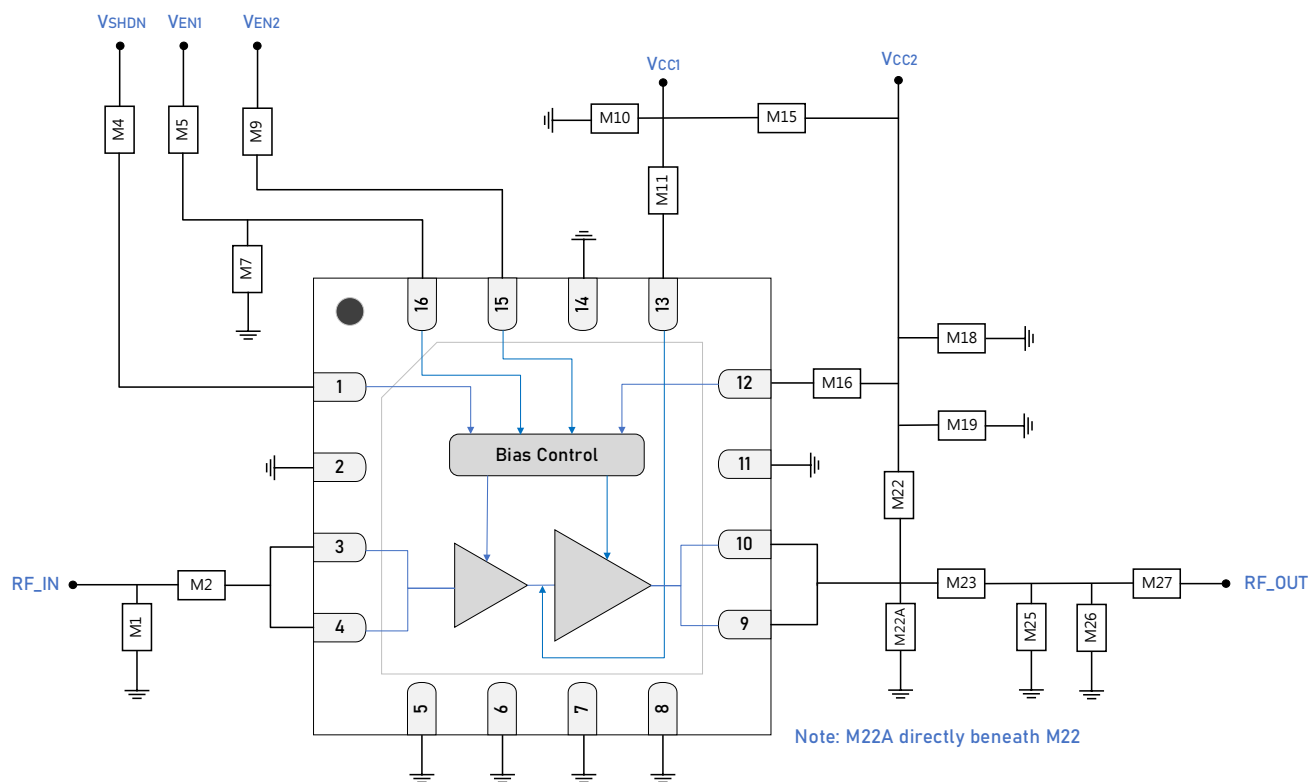
**Note:** Mu factor  $\geq 1.0$  implies unconditional stability.

## GRF5607 Typical Operating Curves: Junction Temperature (per application schematic @ 85 °C)

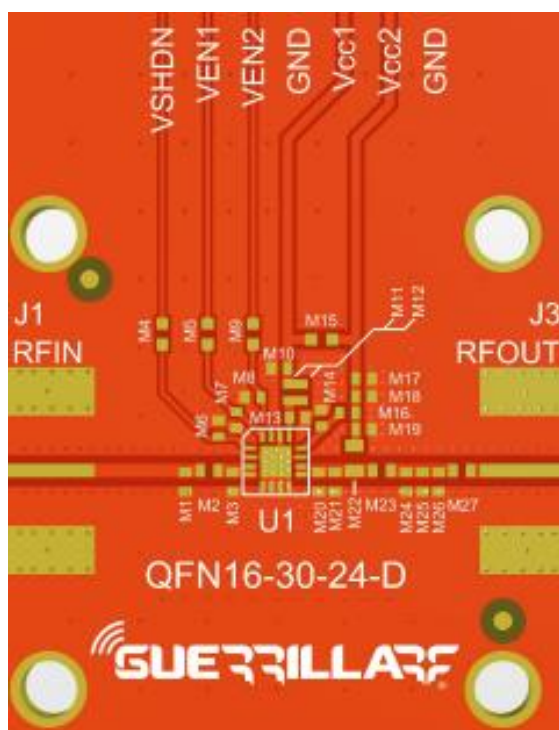
GRF5607, being a 2-stage device, sees one of the stages governing junction temperature over power sweep. Red line = 21 dBm shows where  $T_J$  is equivalent in both stages. At left of red line, stage 1 governs  $T_J$  (Q1  $T_J$  is higher). To the right of red line, stage 2 governs  $T_J$  (Q2  $T_J$  is higher).

Setting bias resistor M5/M9 per application schematic ensures best linearity and yields thermal performance shown in the plot. If the application does not require high IMD3/ACLR linearity, bias resistor can be adjusted higher. This will lower bias point(s) and junction temperature will be contained within/below that shown in the plot.





### GRF5607 Standard Evaluation Board Schematic



### GRF5607 Evaluation Board Assembly Diagram

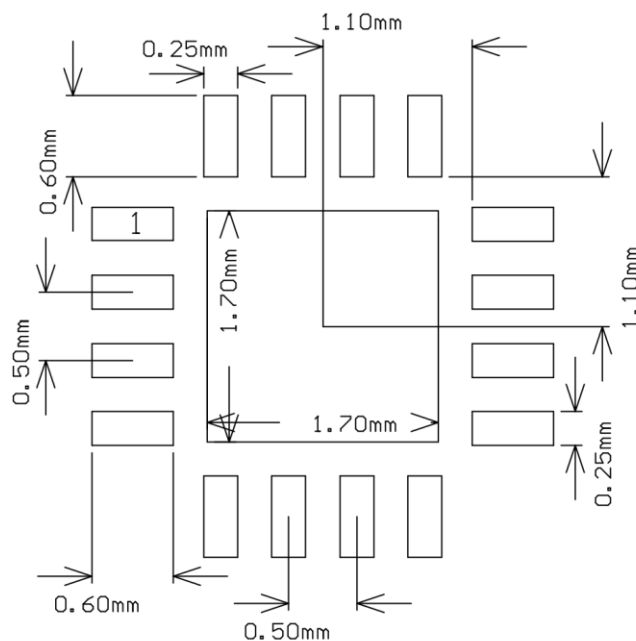
## GRF5607 Evaluation Board Assembly Diagram Reference

| Component        | Type              | Manufacturer | Family    | Value           | Package Size | Substitution |
|------------------|-------------------|--------------|-----------|-----------------|--------------|--------------|
| M1               | Inductor          | Murata       | LQG       | 6.8 nH          | 0402         | ok           |
| M2               | Capacitor         | Murata       | GJM       | 10 pF           | 0402         | ok           |
| M4               | Resistor          | Various      | --        | 0 $\Omega$      | 0402         | ok           |
| M5               | Resistor          | Various      | 1%        | 2.5 k $\Omega$  | 0402         | ok           |
| M7               | Capacitor         | Murata       | GRM       | 100 pF          | 0402         | ok           |
| M9               | Resistor          | Various      | 1%        | 4.55 k $\Omega$ | 0402         | ok           |
| M10              | Capacitor         | Murata       | GRM       | 0.1 $\mu$ F     | 0402         | ok           |
| M11              | Inductor          | CoilCraft    | 0402HP    | 33 nH           | 0402         | ok           |
| M15              | Resistor (jumper) | Various      | --        | 0 $\Omega$      | 0402         | ok           |
| M16              | Resistor          | Various      | --        | 0 $\Omega$      | 0402         | ok           |
| M18              | Capacitor         | Murata       | ** GRM    | 10 $\mu$ F      | 0402         | ok           |
| M19              | Capacitor         | Murata       | GRM       | 100 pF          | 0402         | ok           |
| M22              | Inductor          | Murata       | LQW18AN80 | 24 nH           | 0603         | ok           |
| M22A             | Capacitor         | Murata       | GJM       | 12 pF           | 0402         | ok           |
| M23              | Inductor          | CoilCraft    | 0402HP    | 1.0 nH          | 0402         | ok           |
| M25              | Capacitor         | Murata       | GJM       | 9.1 pF          | 0402         | ok           |
| M26              | Capacitor         | Murata       | GJM       | 2.0 pF          | 0402         | ok           |
| M27              | Capacitor         | Murata       | GRM       | 47 pF           | 0402         | ok           |
| Evaluation Board | QFN16-30-24-D     |              |           |                 |              |              |

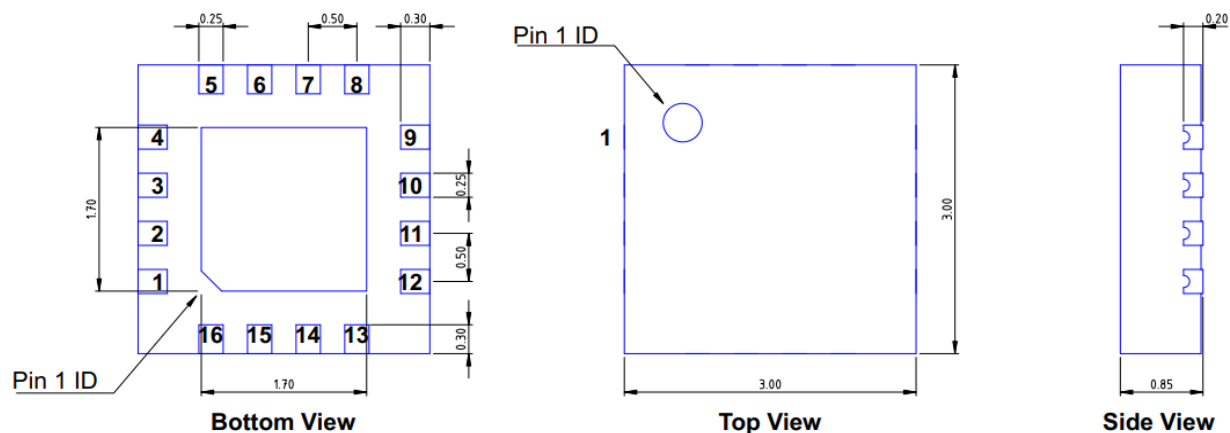
### Notes:

Standard evaluation board bias:  $V_{CC} = 5$  V,  $V_{ENABLE} = 5$  V.

\*\* 10  $\mu$ F must be rated for > 5 V at maximum ambient temperature. Manufacturer Part Number in this case = GRM155C80J106ME11D.



**3 x 3 mm QFN-16 Suggested PCB Footprint (Top View)**



**QFN16 3x3mm**

Dimensions in millimeters  
Dimensional Tolerance:  $\pm 0.05$

**3 x 3 mm QFN-16 Package Dimensions**

## Package Marking Diagram



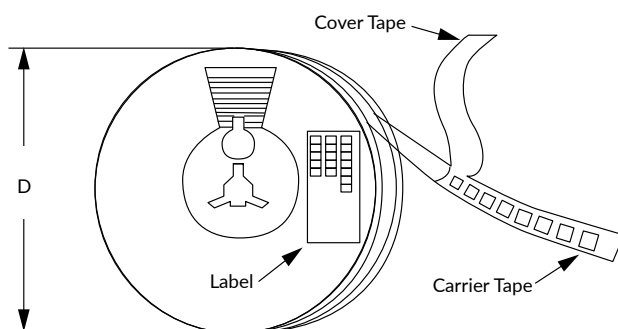
- Line 1: "YY" = YEAR. "WW" = WORK WEEK the device was assembled.
- Line 2: "GRF" = Guerrilla RF.
- Line 3: "XXXX" = Device PART NUMBER.

## Tape and Reel Information

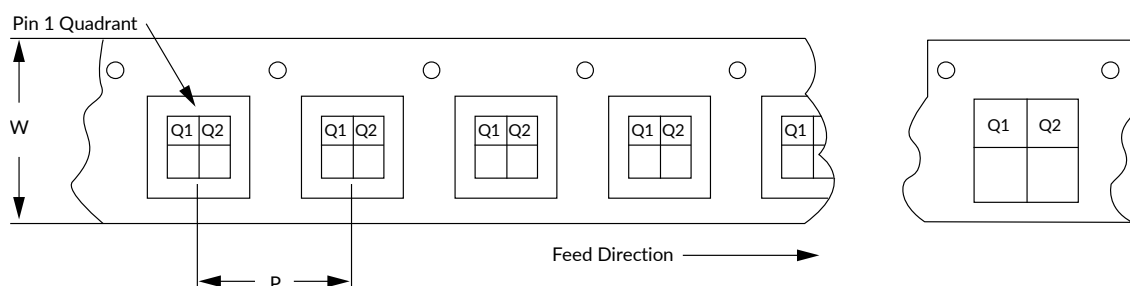
Guerrilla RF's tape and reel specification complies with Electronic Industries Alliance (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). See the following page for the Tape and Reel Specification and Device Package Information table, which includes units per reel.

Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag and the outside surface of the box.

For the Tape and Reel Reference Table, please refer to: <https://www.guerrilla-rf.com/prodFiles/Manufacturing/MN001.pdf>



Tape and Reel Packaging with Reel Diameter Noted (D)



Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information

## Revision History

| Revision Date      | Description of Change                                                                                   |
|--------------------|---------------------------------------------------------------------------------------------------------|
| September 21, 2021 | Preliminary Data Sheet.                                                                                 |
| March 8, 2022      | Updated Package Marking Diagram.                                                                        |
| September 19, 2022 | Changed M9 on evaluation board BOM from 5.62 kΩ to 4.55 kΩ.                                             |
| May 25, 2023       | Release Ø Data Sheet.                                                                                   |
| May 31, 2023       | Appended note referencing M4 on page 4.                                                                 |
| February 15, 2024  | Raised Maximum Junction Temperature to 190 °C. Added Thermal Resistance specifications for Stage 1 & 2. |
| January 23, 2025   | Updated Data Sheet with cosmetic changes only. No change to device or device specifications.            |
| June 11, 2025      | Page 1: updated lower frequency range for GRF5608 and GRF5610.                                          |



## Data Sheet Classifications

| Data Sheet Status | Notes                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Advance           | S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices.                                                                                                                                                                                                      |
| Preliminary       | All data based on limited evaluation board measurements taken within the Guerrilla RF Applications Lab. All parametric values are subject to change pending the collection of additional data.                                                                                                                                                                                                                                   |
| Release Ø         | All data based on measurements taken with <i>production-released</i> material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using <i>modelled estimates</i> that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory. |
| Release A-Z       | All data based on measurements taken with production-released material <i>derived from multiple lots which have been fabricated over an extended period of time</i> . MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads.                                                                                                                   |

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