DATA SHEET

PRELIMINARY DATA SHEET

GRF6412

31.75 dB RANGE / 0.25 dB STEP DIGITAL VGA 0.05 to 8 GHz

FEATURES

- 31.75 dB range with 0.25 dB steps via 7-bit Control
- Serial Interface with Support for 8 Addresses
- Programmable *Rapid Fire*™ Attenuation Setting Which Circumvents Delays Associated with SPI Programming
- Glitchless Stepping (< 2dB Over/Undershoot)
- DSA Supports Bi-directional RF Use
- 3.3 V and 5 V Supply Voltages
- 50 Ω Single-ended Input and Output Impedances
- -40 to 115 °C Operating Temperature Range
- Compact 4 x 4 mm QFN-24 Package

Reference: 5 V / 2 GHz / DSA+AMP Cascade / Max G

- Gain: 19.2 dB
- Noise Figure: 2.6 dB
- OP1dB: 22.9 dBm
- OIP3: 37.0 dBm
- INL Attenuation Error: 0.04 dB
- DNL Attenuation Error: 0.05 dB

Reference: 5 V / 2 GHz / AMP+DSA Cascade / Max G

- Gain: 19 dB
- Noise Figure: 1.8 dB
- OP1dB: 21.7 dBm
- OIP3: 35.7 dBm
- INL Attenuation Error: 0.04 dB
- DNL Attenuation Error: 0.05 dB

APPLICATIONS

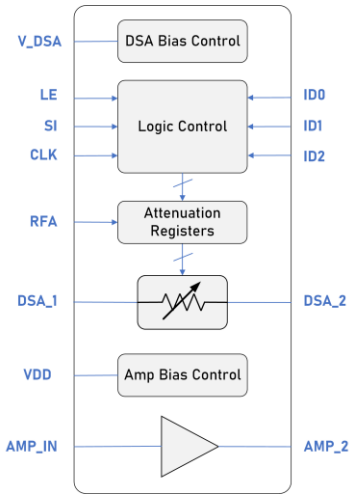
- Wireless Infrastructure
- Automotive Cellular and V2X Compensators
- High Performance Gain Trim & AGC Loops

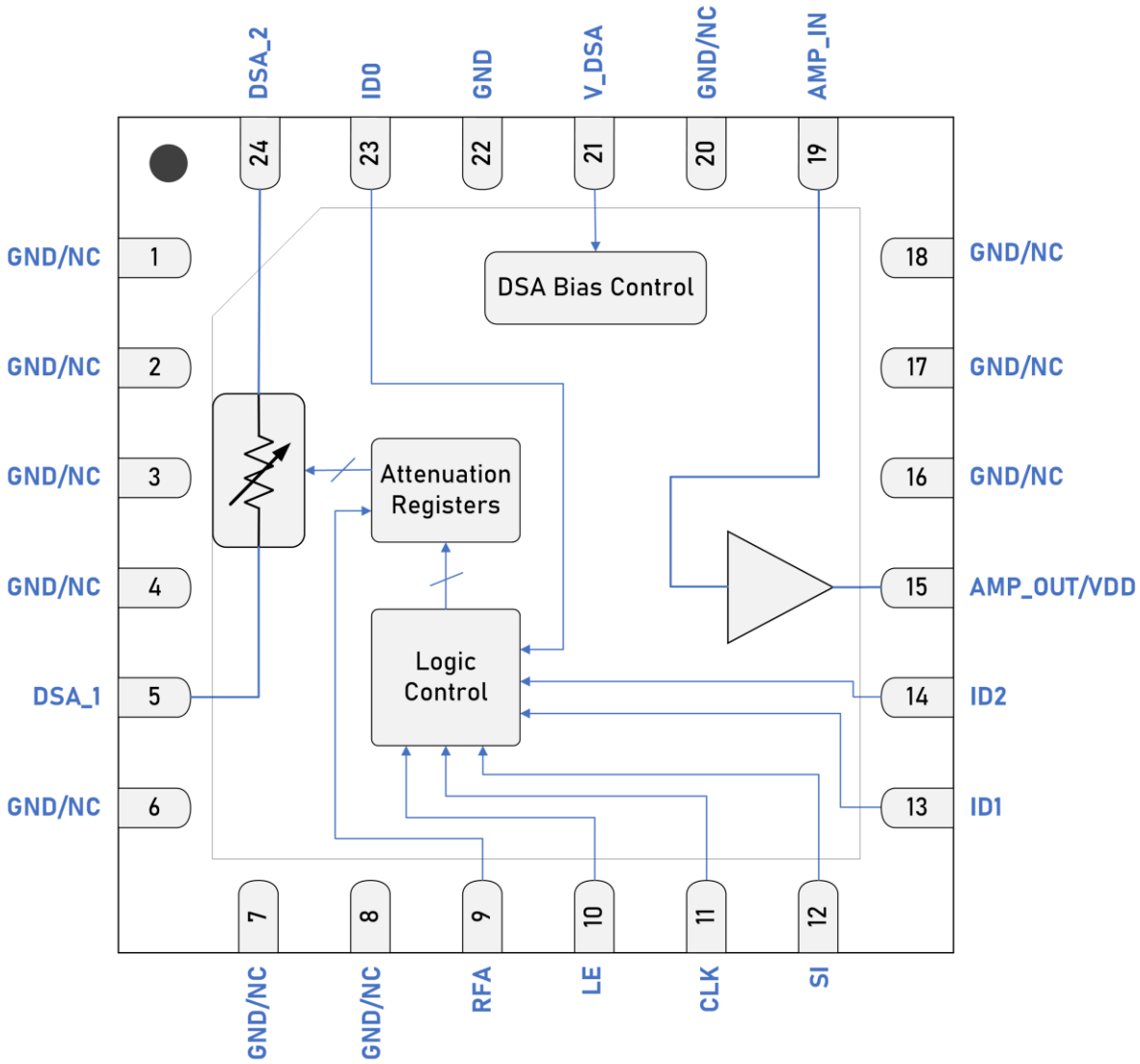
DESCRIPTION

The GRF6412 is a SPI-controlled, 31.75 dB range digital variable gain amplifier (DVGA) which provides precise stepping in 0.25 dB increments. The device's serial interface utilizes three externally defined address bits, allowing up to 8 unique devices to share a common SPI bus. In addition to supporting traditional serial programming, the GRF6412 also includes a special *Rapid Fire*™ selection pin which allows the device to be immediately switched into a pre-defined attenuation state.

In terms of performance, the GRF6412 can cover the entire 50 MHz to 8 GHz range while still maintaining flat gain as well as precise and monotonic gain stepping. Glitching has been minimized to < 2 dB for all steps. The flexibility of the bi-directional attenuator also allows the device to support DSA+AMP as well as AMP+DSA cascaded configurations.

BLOCK DIAGRAM





Pin Out (Top View)

Pin Assignments

Pin	Name	Description	Note
1-4, 6-8, 16-18, 20	GND/NC	Ground or No Connect	No internal connection to die. Although these pins are not connected to the die, they should be grounded with a via as close to the pin as possible.
5	DSA_1	DSA Port 1	Internally matched 50 Ω. An external DC blocking cap must be used if there is voltage present on the RF line. Since the attenuator supports bi-directional operation, the DSA_1 port can serve as an input or output.
9	RFA	Rapid Fire Attenuation Select	Logic control for engaging the "*Rapid Fire Attenuation*" feature. Logic HIGH sets the DSA to the pre-defined RFA attenuation state (which is typically set during the initial SPI programming phase). If a custom attenuation setting is not programmed in, then the RFA setting will default to the full attenuation state (31.75 dB). Logic LOW reverts to the previous attenuation state as defined during the last programming sequence. Refer to the programming section for details.
10	LE	Latch Enable	If left unconnected, logic will default to HIGH due to included pull-up on chip. Logic LOW allows data to be shifted in. The logic transition from LOW to HIGH and then back to LOW updates the programming register.
11	CLK	Clock	Serial clock input.
12	SI	Serial Input	Serial data input.
13	ID1	Chip ID Address Bit 1	External address bit 1. See the programming section for details. If left unconnected, an internal pull-up resistor will force the logic on this pin to HIGH.
14	ID2	Chip ID Address Bit 2	External address bit 2. See the programming section for details. If left unconnected, an internal pull-up resistor will force the logic on this pin to HIGH.
15	AMP_OUT/VDD	Amplifier Output / VDD Bias	Provide device VDD via external bias inductor/ferrite bead.
19	AMP_IN	Amplifier Input	External match must provide DC block.
21	V_{DSA} (V_DSA)	DSA Bias Voltage	Connect to . V_{DD} Use bypass capacitors as close to the pin as possible.
22	GND	Ground	Internally grounded. This pin must be grounded with a via as close to the pin as possible.
23	ID0	Chip ID Address Bit 0	External address bit 0. See the programming section for details. If left unconnected, an internal pull-down resistor of 2000 kΩ will force the logic on this pin to LOW.
24	DSA_2	DSA Port 2	Internally matched 50 Ω. An external DC blocking cap must be used if there is voltage present on the RF line. Since the attenuator supports bi-directional operation, the DSA_2 port can serve as an input or output.
PKG BASE	GND	Ground	Provides DC and RF ground for the amplifier, as well as thermal heat sink. Recommend multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page.

Absolute Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage - DSA	V_{DSA}	-0.3	6	V
Supply Voltage – Amplifier	V_{DD}	-0.3	6	V
SI, LE, CLK	V_{SPI}	-0.3	6	V
ID0, ID1, ID2, RFA	V_{LOGIC}	-0.3	6	V
Externally Applied DC Voltage to DSA_1 Pin	V_{DSA_1}	-0.3	0.3	V
Externally Applied DC Voltage to DSA_2 Pin	V_{DSA_2}	-0.3	0.3	V
Short-term Exposure to RF Input Power - DSA (DSA_1 or DSA_2, Load VSWR = 1:1; Assumes Static State Only; All Attenuation States, V_{DSA} = 5 V, F_{TEST} ≥ 500 MHz, No Hot Switching, $T_{PKG\ BASE}$ = 25 °C).	$P_{DSA\ IN\ MAX\ -\ ST}$		32	dBm
Long-term Exposure to RF Input Power - DSA (DSA_1 or DSA_2, Load VSWR = 1:1; Assumes Static State Only; Max Attenuation State (31.75 dB), V_{DSA} = 5.5 V, F_{TEST} = 50 MHz, No Hot Switching, $T_{PKG\ BASE}$ = 105 °C).	$P_{DSA\ IN\ MAX\ -\ LT}$		26.5	dBm
Long-term Exposure to RF Input Power – Amplifier (CW, Load VSWR < 2:1, VDD = 5 V).	$P_{AMP\ IN\ MAX\ -\ LT}$		TBD	dBm
Operating Temperature (Exposed Paddle on Package Base)	$T_{PKG\ BASE}$	-40	115	°C
Maximum Junction Temperature – DSA Core	$T_{J\text{-}MAX}$		125	°C
Maximum Channel Temperature – Amplifier Core	$T_{CH\text{-}MAX}$		170	°C
Electrostatic Discharge				
Charged Device Model	CDM	TBD		kV
Human Body Model	HBM	TBD		kV
Storage				
Storage Temperature	T_{STG}	-65	150	°C
Moisture Sensitivity Level	MSL		1	--

Caution! ESD Sensitive Device.
Exceeding Absolute Maximum Rating conditions may cause permanent damage.

Note: For additional information, please refer to *Manufacturing Note MN-001 — Package and Manufacturing Information.*

All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging. For additional information, please refer to the *Certificate of RoHS Compliance.*

Recommended Operating Conditions

Parameter		Symbol	Specification			Unit	Condition
			Min.	Typ.	Max.		
Power Supply Voltage - DSA		V_{DSA}	3	5	5.5	V	
Power Supply Voltage - Amplifier		V_{DD}	3	5	6	V	
Operating Temperature Range		$T_{PKG\ BASE}$	-40		+115	°C	Measured on Package Base.
RF Frequency Range **(note 1)**		F_{RF}	0.05		8	GHz	
RF Input Power – DSA Core	Static States	$P_{IN\ MAX\ -\ DSA}$			27	dBm	Static attenuation state: all state changes occur in the absence of any RF power being applied to the device.
	Hot Switching				20		Hot switching condition: state changes can occur at any time while RF power is applied to the device.
RF Input Power – Amplifier Core		$P_{IN\ MAX\ -\ AMP}$			*TBD*	dBm	
DSA_1 Port Impedance		Z_{DSA_1}		50		Ω	Single-ended.
DSA_2 Port Impedance		Z_{DSA_2}		50		Ω	Single-ended.
AMP_IN Port Impedance		Z_{AMP_IN}		50		Ω	Single-ended.
AMP_OUT Port Impedance		Z_{AMP_OUT}		50		Ω	Single-ended.

Note 1: Operation outside of this range is possible, but with degraded performance of some parameters.

Nominal Operating Parameters - General

Parameter		Symbol	Specification			Unit	Condition
			Min.	Typ.	Max.		
Logic Input Low		V_{IL}	0		0.63	V	
Logic Input High		V_{IH}	1.17		V_{DD}	V	
Logic Current		I_{IL}, I_{IH}		200		µA	V_{DSA} = 5 V, $T_{PKG\ BASE}$ = 105 °C.
DSA Supply Current	5 V Supply	I_{DSA-5V}		190		µA	V_{DSA} = 5 V, Static operation
	3.3 V Supply	$I_{DSA-3.3V}$		225		µA	V_{DSA} = 3.3 V, Static operation
Amplifier Supply Current	5 V Supply	I_{AMP-5V}		130		mA	V_{DD} = 5 V
	3.3 V Supply	$I_{AMP-3.3V}$		72		mA	V_{DD} = 3.3 V
Serial Clock Speed		f_{CLK}			30	MHz	
LE to First Serial Clock Rising Edge		t_{LS}	10			ns	50% of LE falling edge to 50% of CLK rising edge.
Serial Data Hold Time		t_H	10			ns	50% of CLK rising edge to 50% of Data falling edge.
Final Serial Clock Rising Edge to LE		t_{CLS}	10			ns	50% of CLK rising edge to 50% of LE rising edge.
DSA Settling Time	Any Adjacent Step	$T_{SETTLE-ADJ}$		47		ns	50% of LE to within 0.1dB of the final value.
	Max to Min Attenuation	$T_{SETTLE-MAX-MIN}$		322		ns	
	Min to Max Attenuation	$T_{SETTLE-MIN-MAX}$		723		ns	

Thermal Data

DSA Thermal Resistance (Infrared Scan)		Θ_{JC-DSA}		47.8		°C/W	On Standard Evaluation Board
Amp Thermal Resistance (Infrared Scan)		Θ_{JC-AMP}		TBD		°C/W	On Standard Evaluation Board
DSA Junction Temperature @ $T_{PKG\ BASE}$ = +115 °C Ref (Pkg Base)		T_J		125		°C	V_{DSA} = 5.5 V, F_{TEST} = 50 MHz, Max Attenuation (31.75 dB), P_{IN} = 23 dBm, CW.
DSA Junction Temperature @ $T_{PKG\ BASE}$ = +105 °C Ref (Pkg Base)		$T_{J\ @\ 105°C}$		115		°C	V_{DSA} = 5.5 V, F_{TEST} = 50 MHz, Max Attenuation (31.75 dB), P_{IN} = 23 dBm, CW.
Amp Channel Temperature @ $T_{PKG\ BASE}$ = +115 °C Ref (Pkg Base)		T_{CH}		TBD		°C	VDD = 5.5 V, F_{TEST} = 50 MHz, P_{IN} = TBD dBm, CW.
Amp Channel Temperature @ $T_{PKG\ BASE}$ = +105 °C Ref (Pkg Base)		$T_{CH\ @\ 105°C}$		TBD		°C	VDD = 5.5 V, F_{TEST} = 50 MHz, P_{IN} = TBD dBm, CW.

Nominal Operating Parameters – RF [DSA → AMP Configuration]

The following conditions apply unless noted otherwise: Typical Application Schematic, **DSA + AMP cascaded in series**, attenuator set for maximum gain (0 dB attenuation), V_{DSA} = 5 V, V_{DD} = 5 V, 50 Ω system impedance, F_{TEST} = 2.0 GHz, $T_{PKG\ BASE}$ = 25 °C. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Gain (DSA + Amp, Cascaded)	G		20.9		dB	F_{RF} = 0.5 GHz
			20.4			F_{RF} = 1 GHz
			19.2			F_{RF} = 2 GHz
			18.7			F_{RF} = 2.5 GHz
			17			F_{RF} = 3.55 GHz
			15.7			F_{RF} = 4.7 GHz
			14.2			F_{RF} = 6.4 GHz
			10.6			F_{RF} = 7.2 GHz
			8.7			F_{RF} = 8 GHz
Gain Flatness Over any 200 MHz Band (DSA + Amp, Cascaded)	G_{FLAT}		0.2		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			0.25			2 GHz ≤ F_{RF} ≤ 3 GHz
			0.4			3 GHz ≤ F_{RF} ≤ 4 GHz
			0.35			4 GHz ≤ F_{RF} ≤ 5 GHz
			0.15			5 GHz ≤ F_{RF} ≤ 6 GHz
			0.35			6 GHz ≤ F_{RF} ≤ 7 GHz
			0.35			7 GHz ≤ F_{RF} ≤ 8 GHz
Gain Variation Over Temp (DSA + Amp, Cascaded)	G_{TEMP}		+0.8 / -0.7		dB	$T_{PKG\ BASE}$ = -40 to 115 °C, Referenced to $T_{PKG\ BASE}$ = 25 °C

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
DSA_1 (Input) Return Loss	RL_{IN}		> 11		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			> 12			2 GHz ≤ F_{RF} ≤ 3 GHz
			> 10			3 GHz ≤ F_{RF} ≤ 4 GHz
			> 9			4 GHz ≤ F_{RF} ≤ 5 GHz
			> 11			5 GHz ≤ F_{RF} ≤ 6 GHz
			>9			6 GHz ≤ F_{RF} ≤ 7 GHz
			>9			7 GHz ≤ F_{RF} ≤ 8 GHz
AMP_OUT (Output) Return Loss	RL_{OUT}		>15		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			>14			2 GHz ≤ F_{RF} ≤ 3 GHz
			>17			3 GHz ≤ F_{RF} ≤ 4 GHz
			>15			4 GHz ≤ F_{RF} ≤ 5 GHz
			>15			5 GHz ≤ F_{RF} ≤ 6 GHz
			>9			6 GHz ≤ F_{RF} ≤ 7 GHz
			>8			7 GHz ≤ F_{RF} ≤ 8 GHz
NF (DSA + Amp, Cascaded)	NF		2.7		dB	F_{RF} = 0.5 GHz
			2.7			F_{RF} = 1 GHz
			2.6			F_{RF} = 2 GHz
			3			F_{RF} = 2.5 GHz
			3.9			F_{RF} = 3.55 GHz
			4.3			F_{RF} = 4.7 GHz
			4			F_{RF} = 6.4 GHz
			6.7			F_{RF} = 7.2 GHz
			7.5			F_{RF} = 8 GHz

Parameter	Symbol	Specification			Unit	Condition	
		Min.	Typ.	Max.			
Output 3rd Order Intercept (DSA + Amp, Cascaded)	OIP3		38		dBm	F_{RF} = 0.5 GHz	4 dBm P_{OUT} per Tone at 1 MHz Spacing ATTN = 0 dB
			38			F_{RF} = 1 GHz	
			37			F_{RF} = 2 GHz	
			37			F_{RF} = 2.5 GHz	
			37			F_{RF} = 3.55 GHz	
			35			F_{RF} = 4.7 GHz	
			34			F_{RF} = 6.4 GHz	
			30			F_{RF} = 7.2 GHz	
			28			F_{RF} = 8 GHz	
			37			ATTN = 0 dB	4 dBm P_{OUT} per Tone at 1 MHz Spacing F_{RF} = 2 GHz
			37			ATTN = 15.75 dB	
			37			ATTN = 31.75 dB	
Output 1dB Compression (DSA + AMP, Cascaded)	OP_{1dB}		22.7		dBm	F_{RF} = 0.5 GHz	ATTN = 0 dB
			22.7			F_{RF} = 1 GHz	
			22.9			F_{RF} = 2 GHz	
			23.1			F_{RF} = 2.5 GHz	
			23			F_{RF} = 3.55 GHz	
			22.4			F_{RF} = 4.7 GHz	
			21			F_{RF} = 6.4 GHz	
			18.2			F_{RF} = 7.2 GHz	
			14.3			F_{RF} = 8 GHz	
			23			ATTN = 0 dB	F_{RF} = 2 GHz
			23			ATTN = 15.75 dB	
			15			ATTN = 31.75 dB	
Attenuation Range	G_{RANGE}		31.75		dB		
Attenuation Resolution	G_{STEP}		0.25		dB		
Over/Undershoot During Step Transition	$G_{OVER/UNDERSHOOT}$		< 2		dB	Any step.	

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Step Error Between Any Two Adjacent States	DNL		± 0.02		dB	0.05 GHz ≤ F_{RF} ≤ 1 GHz
			± 0.03			1 GHz ≤ F_{RF} ≤ 2 GHz
			± 0.05			2 GHz ≤ F_{RF} ≤ 3 GHz
			± 0.07			3 GHz ≤ F_{RF} ≤ 4 GHz
			± 0.08			4 GHz ≤ F_{RF} ≤ 5 GHz
			± 0.09			5 GHz ≤ F_{RF} ≤ 6 GHz
			TBD			6 GHz ≤ F_{RF} ≤ 7 GHz
			TBD			7 GHz ≤ F_{RF} ≤ 8 GHz
Absolute Attenuation Error at 0.5 GHz	$INL_{0.5\ GHz}$		0.07		dB	ATTN = 6 dB
			0.11			ATTN = 10 dB
			0.18			ATTN = 18 dB
			0.24			ATTN = 24 dB
			0.26			ATTN = 30 dB
Absolute Attenuation Error at 1 GHz	$INL_{1\ GHz}$		0.05		dB	ATTN = 6 dB
			0.09			ATTN = 10 dB
			0.13			ATTN = 18 dB
			0.17			ATTN = 24 dB
			0.15			ATTN = 30 dB
Absolute Attenuation Error at 2 GHz	$INL_{2\ GHz}$		0.03		dB	ATTN = 6 dB
			0.04			ATTN = 10 dB
			0.04			ATTN = 18 dB
			0.02			ATTN = 24 dB
			-0.03			ATTN = 30 dB

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Absolute Attenuation Error at 2.5 GHz	INL 2.5 GHz		0.02		dB	ATTN = 6 dB
			0.01			ATTN = 10 dB
			-0.05			ATTN = 18 dB
			-0.12			ATTN = 24 dB
			-0.27			ATTN = 30 dB
Absolute Attenuation Error at 3.55 GHz	INL 3.55 GHz		0.01		dB	ATTN = 6 dB
			-0.03			ATTN = 10 dB
			-0.19			ATTN = 18 dB
			-0.37			ATTN = 24 dB
			-0.66			ATTN = 30 dB
Absolute Attenuation Error at 4.7 GHz	INL 4.7 GHz		0.03		dB	ATTN = 6 dB
			-0.06			ATTN = 10 dB
			-0.38			ATTN = 18 dB
			-0.72			ATTN = 24 dB
			-1.18			ATTN = 30 dB
Absolute Attenuation Error at 6.4 GHz	INL 6.4 GHz		0.03		dB	ATTN = 6 dB
			-0.06			ATTN = 10 dB
			-0.38			ATTN = 18 dB
			-0.72			ATTN = 24 dB
			-1.18			ATTN = 30 dB
Absolute Attenuation Error at 7.2 GHz	INL 7.2 GHz		TBD		dB	ATTN = 6 dB
			TBD			ATTN = 10 dB
			TBD			ATTN = 18 dB
			TBD			ATTN = 24 dB
			TBD			ATTN = 30 dB

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Absolute Attenuation Error at 8 GHz	$INL_{8\ GHz}$		TBD		dB	ATTN = 6 dB
			TBD			ATTN = 10 dB
			TBD			ATTN = 18 dB
			TBD			ATTN = 24 dB
			TBD			ATTN = 30 dB
Relative Phase Between the MIN and MAX Attenuation States	Φ_{Δ}		7		°	F_{RF} = 0.5 GHz
			12.5			F_{RF} = 1 GHz
			25			F_{RF} = 2 GHz
			31			F_{RF} = 2.5 GHz
			42			F_{RF} = 3.55 GHz
			54			F_{RF} = 4.7 GHz
			68			F_{RF} = 6.4 GHz
			TBD			F_{RF} = 7.2 GHz
			TBD			F_{RF} = 8 GHz
Adjacent Step Phase Deviation at 0.5 GHz	$ASPD_{0.5\ GHz}$		0.13		°	ATTN = 6 dB
			0.09			ATTN = 10 dB
			0.11			ATTN = 18 dB
			0.33			ATTN = 24 dB
			0.4			ATTN = 30 dB
Adjacent Step Phase Deviation at 1 GHz	$ASPD_{1\ GHz}$		0.22		°	ATTN = 6 dB
			0.2			ATTN = 10 dB
			0.23			ATTN = 18 dB
			0.53			ATTN = 24 dB
			0.58			ATTN = 30 dB

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Adjacent Step Phase Deviation at 2 GHz	$ASPD_{2\ GHz}$		0.42		°	ATTN = 6 dB
			0.45			ATTN = 10 dB
			0.54			ATTN = 18 dB
			1.04			ATTN = 24 dB
			0.89			ATTN = 30 dB
Adjacent Step Phase Deviation at 2.5 GHz	$ASPD_{2.5\ GHz}$		0.54		°	ATTN = 6 dB
			0.59			ATTN = 10 dB
			0.72			ATTN = 18 dB
			1.29			ATTN = 24 dB
			1.11			ATTN = 30 dB
Adjacent Step Phase Deviation at 3.55 GHz	$ASPD_{3.55\ GHz}$		0.84		°	ATTN = 6 dB
			0.92			ATTN = 10 dB
			1.1			ATTN = 18 dB
			1.89			ATTN = 24 dB
			1.45			ATTN = 30 dB
Adjacent Step Phase Deviation at 4.7 GHz	$ASPD_{4.7\ GHz}$		1.18		°	ATTN = 6 dB
			1.31			ATTN = 10 dB
			1.55			ATTN = 18 dB
			2.47			ATTN = 24 dB
			1.89			ATTN = 30 dB
Adjacent Step Phase Deviation at 6.4 GHz	$ASPD_{6.4\ GHz}$		1.55		°	ATTN = 6 dB
			1.69			ATTN = 10 dB
			2.04			ATTN = 18 dB
			3.11			ATTN = 24 dB
			2.52			ATTN = 30 dB

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Adjacent Step Phase Deviation at 7.2 GHz	$ASPD_{7.2\ GHz}$		TBD		°	ATTN = 6 dB
			TBD			ATTN = 10 dB
			TBD			ATTN = 18 dB
			TBD			ATTN = 24 dB
			TBD			ATTN = 30 dB
Adjacent Step Phase Deviation at 8 GHz	$ASPD_{8\ GHz}$		TBD		°	ATTN = 6 dB
			TBD			ATTN = 10 dB
			TBD			ATTN = 18 dB
			TBD			ATTN = 24 dB
			TBD			ATTN = 30 dB
Maximum Non-RF Driven Spurious Over Rated Frequency Range of 50 MHz to 8 GHz **(note 2)**	$Spur_{MAX}$		TBD		dBm	F_{RF} = 50 MHz to 65 MHz
			TBD			F_{RF} = 65 MHz to 115 MHz
			TBD			F_{RF} = 115 MHz to 8 GHz

Note 2: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 10 MHz. Measured at AMP_OUT port, terminated into 50 Ω. DSA + Amp cascaded.

Nominal Operating Parameters – RF [AMP → DSA Configuration]

The following conditions apply unless noted otherwise: Typical Application Schematic, **AMP + DSA cascaded in series**, attenuator set for maximum gain (0 dB attenuation), V_{DSA} = 5 V, V_{DD} = 5 V, 50 Ω system impedance, F_{TEST} = 2.0 GHz, $T_{PKG\ BASE}$ = 25 °C. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Gain (AMP + DSA, Cascaded)	G		21		dB	F_{RF} = 0.5 GHz
			20.5			F_{RF} = 1 GHz
			19			F_{RF} = 2 GHz
			18.7			F_{RF} = 2.5 GHz
			17			F_{RF} = 3.55 GHz
			15.7			F_{RF} = 4.7 GHz
			14.2			F_{RF} = 6.4 GHz
			11			F_{RF} = 7.2 GHz
			9			F_{RF} = 8 GHz
Gain Flatness Over any 200 MHz Band (AMP + DSA, Cascaded)	G_{FLAT}		0.2		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			0.25			2 GHz ≤ F_{RF} ≤ 3 GHz
			0.4			3 GHz ≤ F_{RF} ≤ 4 GHz
			0.35			4 GHz ≤ F_{RF} ≤ 5 GHz
			0.15			5 GHz ≤ F_{RF} ≤ 6 GHz
			0.20			6 GHz ≤ F_{RF} ≤ 7 GHz
			0.30			7 GHz ≤ F_{RF} ≤ 8 GHz
Gain Variation Over Temp (AMP + DSA, Cascaded)	G_{TEMP}		+0.8 / -0.7		dB	$T_{PKG\ BASE}$ = -40 to 115 °C, Referenced to $T_{PKG\ BASE}$ = 25 °C

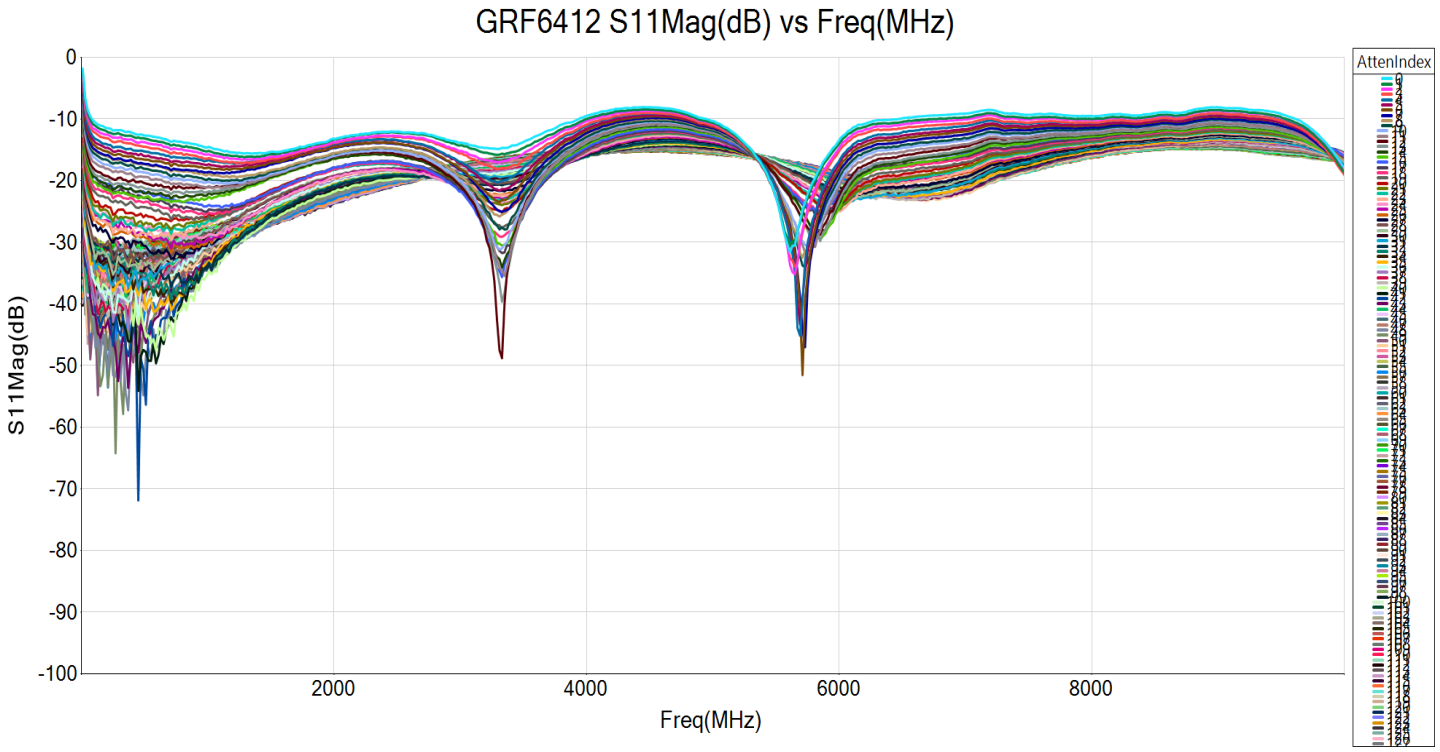
Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
AMP_IN (Input) Return Loss	RL_{IN}		> 8.5		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			> 9			2 GHz ≤ F_{RF} ≤ 3 GHz
			> 9			3 GHz ≤ F_{RF} ≤ 4 GHz
			> 9			4 GHz ≤ F_{RF} ≤ 5 GHz
			> 10			5 GHz ≤ F_{RF} ≤ 6 GHz
			>9			6 GHz ≤ F_{RF} ≤ 7 GHz
			>12			7 GHz ≤ F_{RF} ≤ 8 GHz
DSA_2 (Output) Return Loss	RL_{OUT}		> 22		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			> 20			2 GHz ≤ F_{RF} ≤ 3 GHz
			> 20			3 GHz ≤ F_{RF} ≤ 4 GHz
			> 18			4 GHz ≤ F_{RF} ≤ 5 GHz
			> 15			5 GHz ≤ F_{RF} ≤ 6 GHz
			>8			6 GHz ≤ F_{RF} ≤ 7 GHz
			>9			7 GHz ≤ F_{RF} ≤ 8 GHz
NF (AMP + DSA, Cascaded)	NF		1.2		dB	F_{RF} = 0.5 GHz
			1.5			F_{RF} = 1 GHz
			1.8			F_{RF} = 2 GHz
			1.8			F_{RF} = 2.5 GHz
			1.9			F_{RF} = 3.55 GHz
			1.9			F_{RF} = 4.7 GHz
			2			F_{RF} = 6.4 GHz
			2.5			F_{RF} = 7.2 GHz
			3.0			F_{RF} = 8 GHz

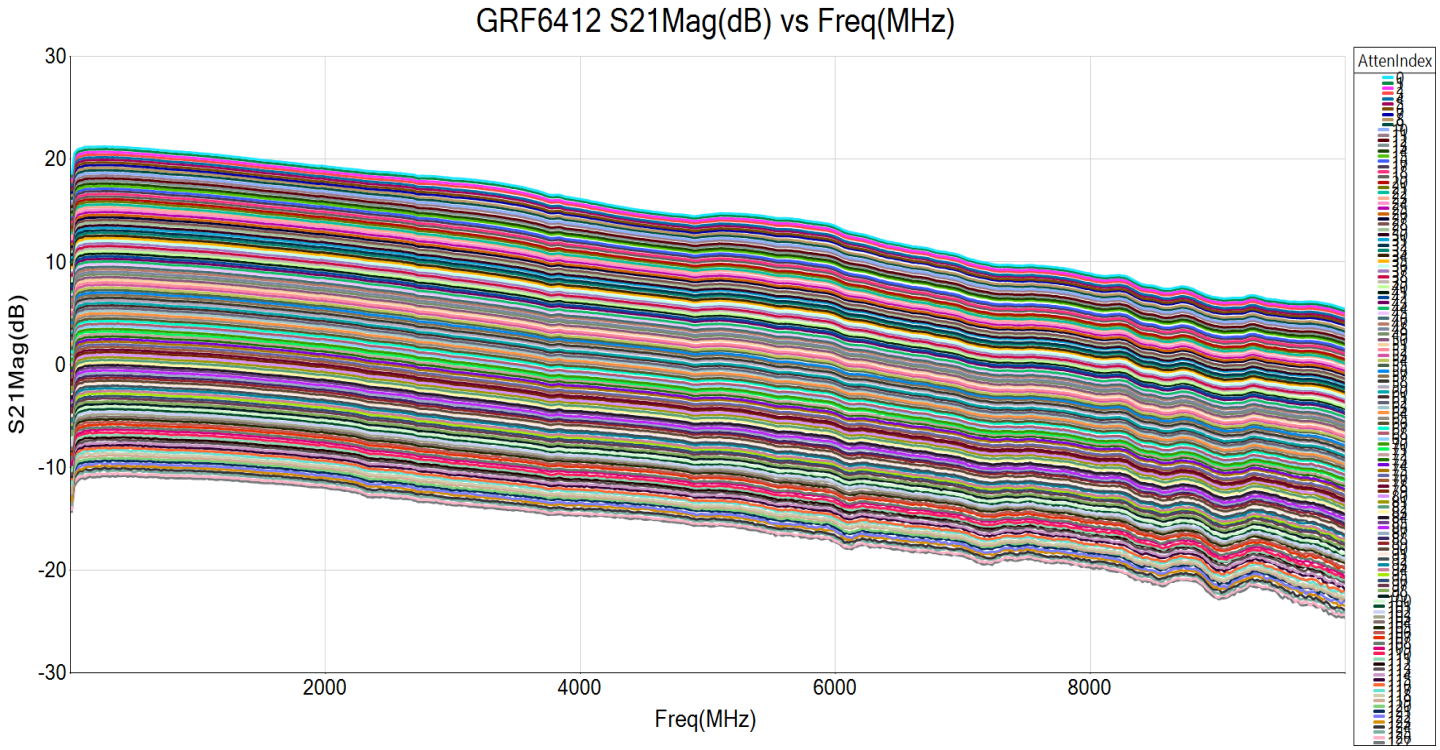
Parameter	Symbol	Specification			Unit	Condition	
		Min.	Typ.	Max.			
Output 3rd Order Intercept (AMP + DSA, Cascaded)	OIP3		36.9		dBm	F_{RF} = 0.5 GHz	4 dBm P_{OUT} per Tone at 1 MHz Spacing ATTN = 0 dB
			36.8			F_{RF} = 1 GHz	
			35.7			F_{RF} = 2 GHz	
			35.6			F_{RF} = 2.5 GHz	
			34.4			F_{RF} = 3.55 GHz	
			33			F_{RF} = 4.7 GHz	
			31.4			F_{RF} = 6.4 GHz	
			28			F_{RF} = 7.2 GHz	
			25			F_{RF} = 8 GHz	
			37			ATTN = 0 dB	4 dBm P_{OUT} per Tone at 1 MHz Spacing F_{RF} = 2 GHz
			19			ATTN = 15.75 dB	
			4			ATTN = 31.75 dB	
Output 1dB Compression (AMP + DSA, Cascaded)	OP_{1dB}		21.4		dBm	F_{RF} = 0.5 GHz	ATTN = 0 dB
			21.4			F_{RF} = 1 GHz	
			21.7			F_{RF} = 2 GHz	
			21.6			F_{RF} = 2.5 GHz	
			20.9			F_{RF} = 3.55 GHz	
			20			F_{RF} = 4.7 GHz	
			18.5			F_{RF} = 6.4 GHz	
			14			F_{RF} = 7.2 GHz	
			10			F_{RF} = 8 GHz	
			23			ATTN = 0 dB	F_{RF} = 2 GHz
			5.4			ATTN = 15.75 dB	
			-10			ATTN = 31.75 dB	
Attenuation Range	G_{RANGE}		31.75		dB		
Attenuation Resolution	G_{STEP}		0.25		dB		
Over/Undershoot During Step Transition	$G_{OVER/UNDERSHOOT}$		< 2		dB	Any step.	

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Maximum Non-RF Driven Spurious Over Rated Frequency Range of 50 MHz to 8 GHz **(note 3)**	$Spur_{MAX}$		TBD		dBm	F_{RF} = 50 MHz to 65 MHz
			TBD			F_{RF} = 65 MHz to 115 MHz
			TBD			F_{RF} = 115 MHz to 8 GHz

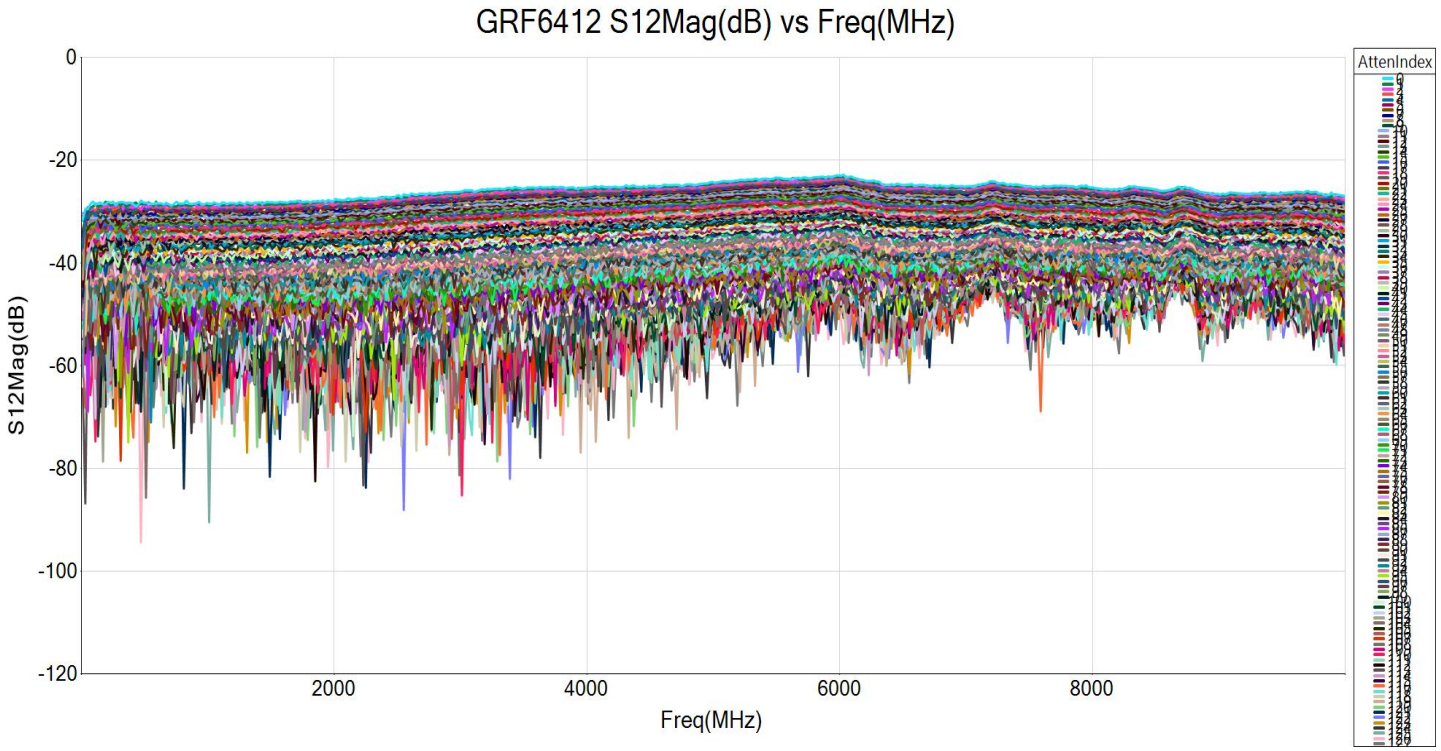
Note 3: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 10 MHz. Measured at DSA_2 port, terminated into 50 Ω. AMP + DSA cascaded.

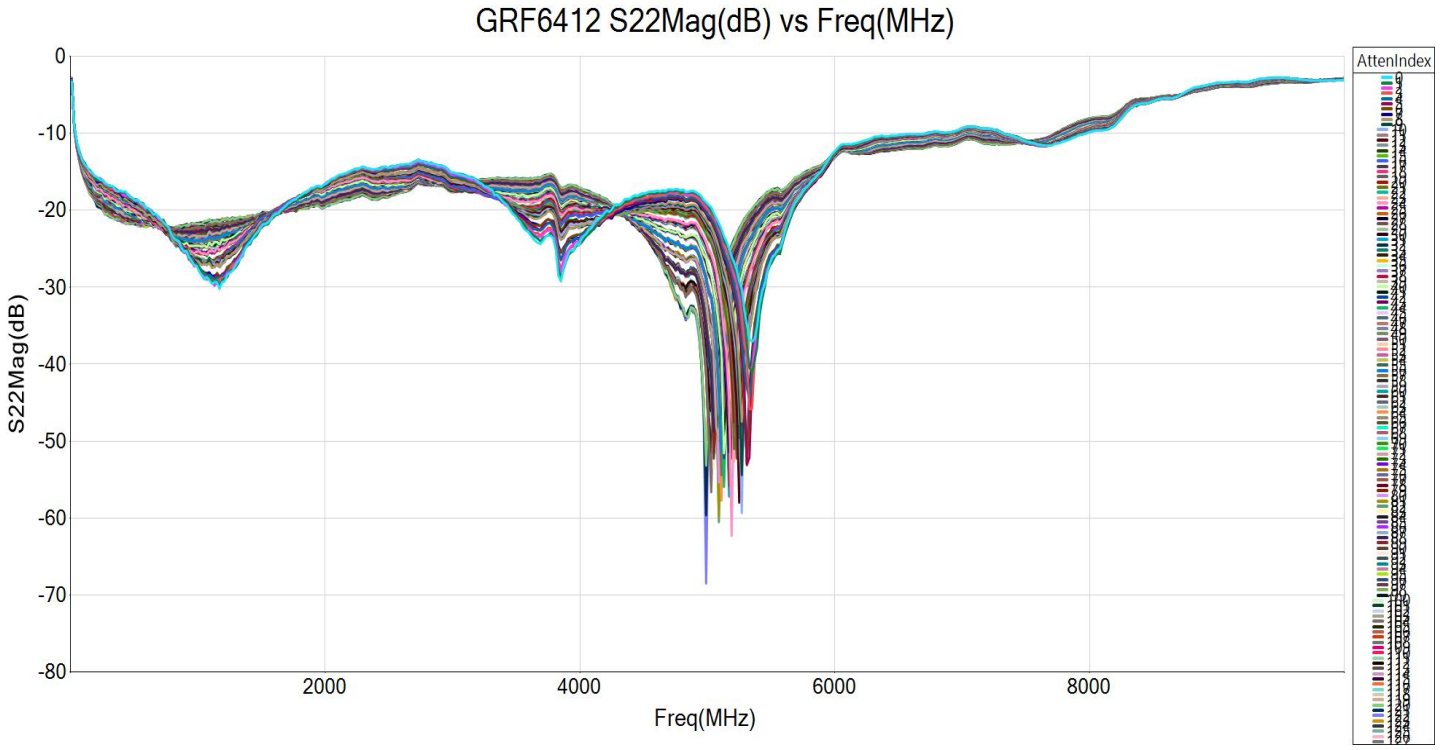
GRF6412 Typical Operating Curves: S-Parameters (DSA to AMP)



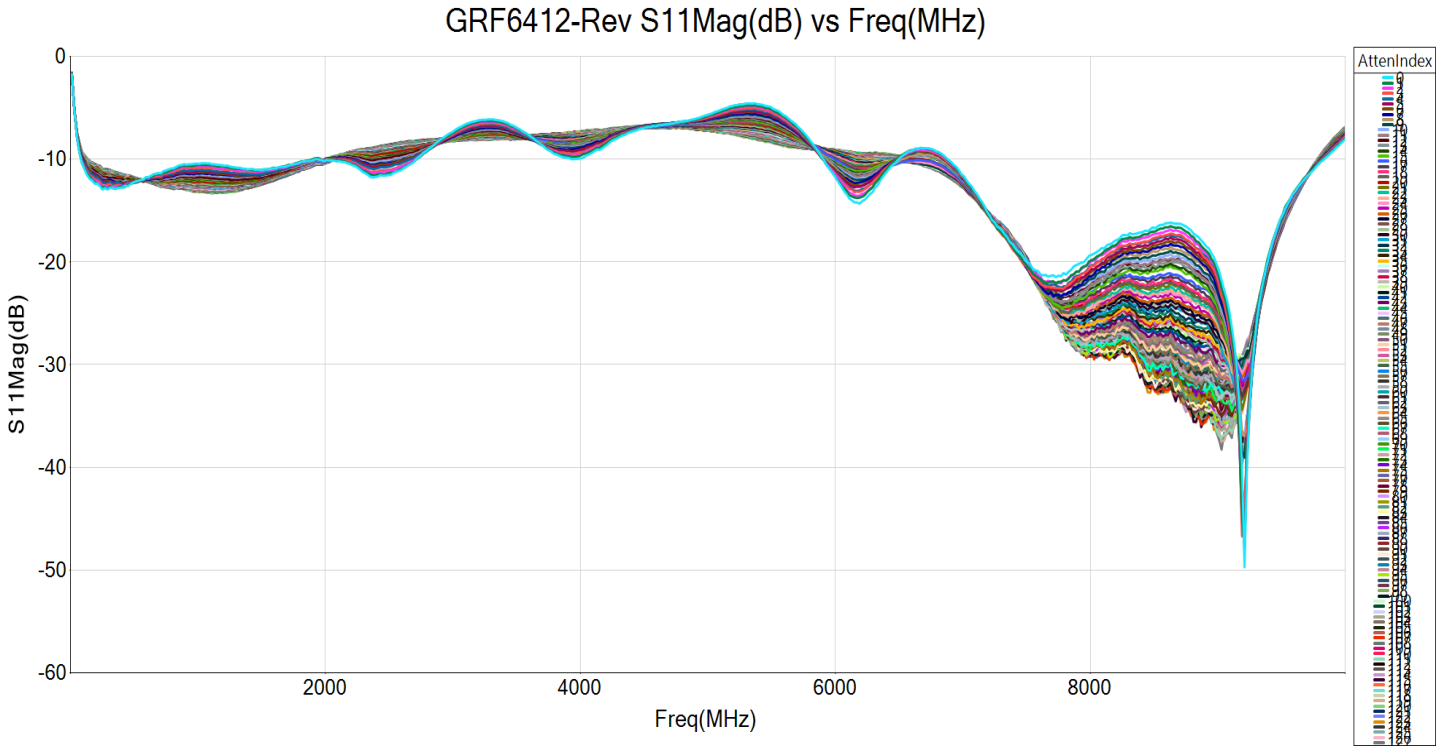


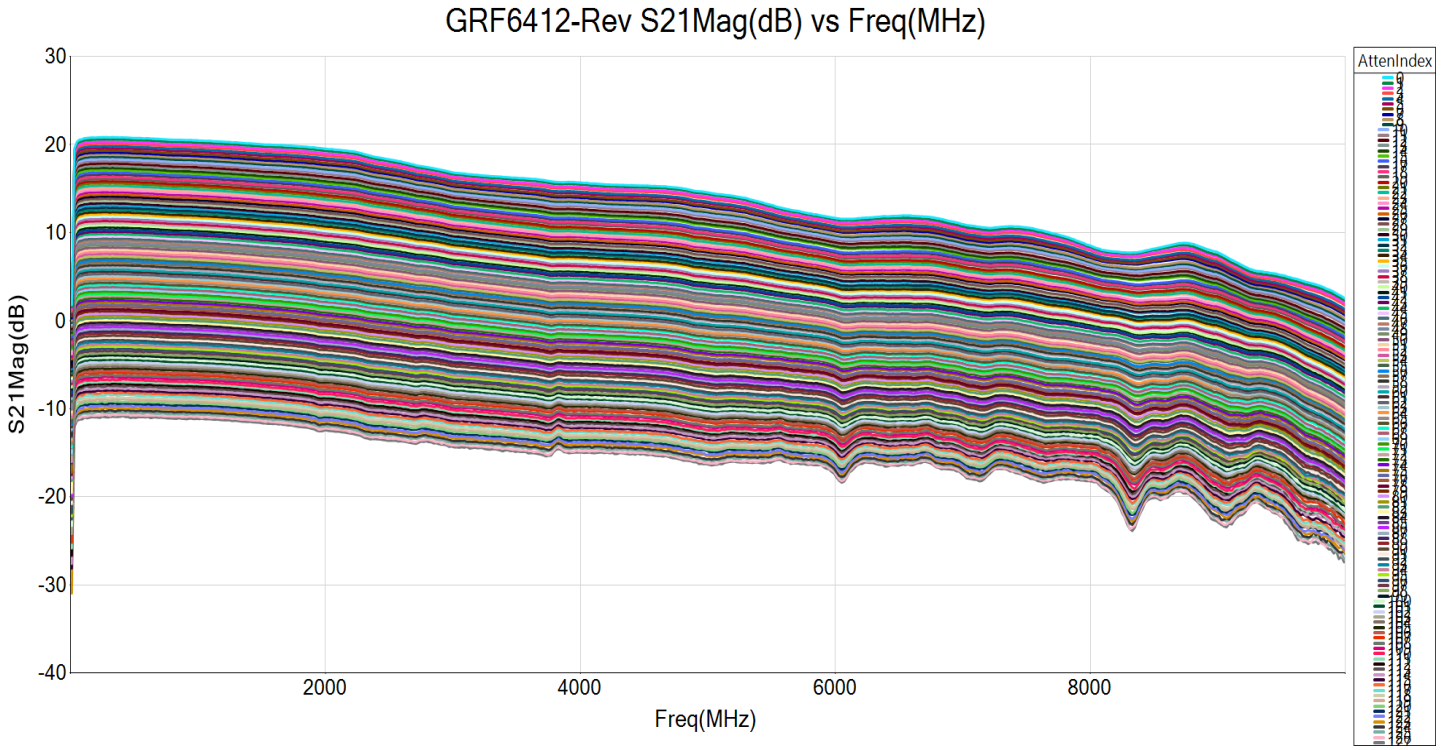
GRF6412 Typical Operating Curves: S-Parameters (DSA to AMP)



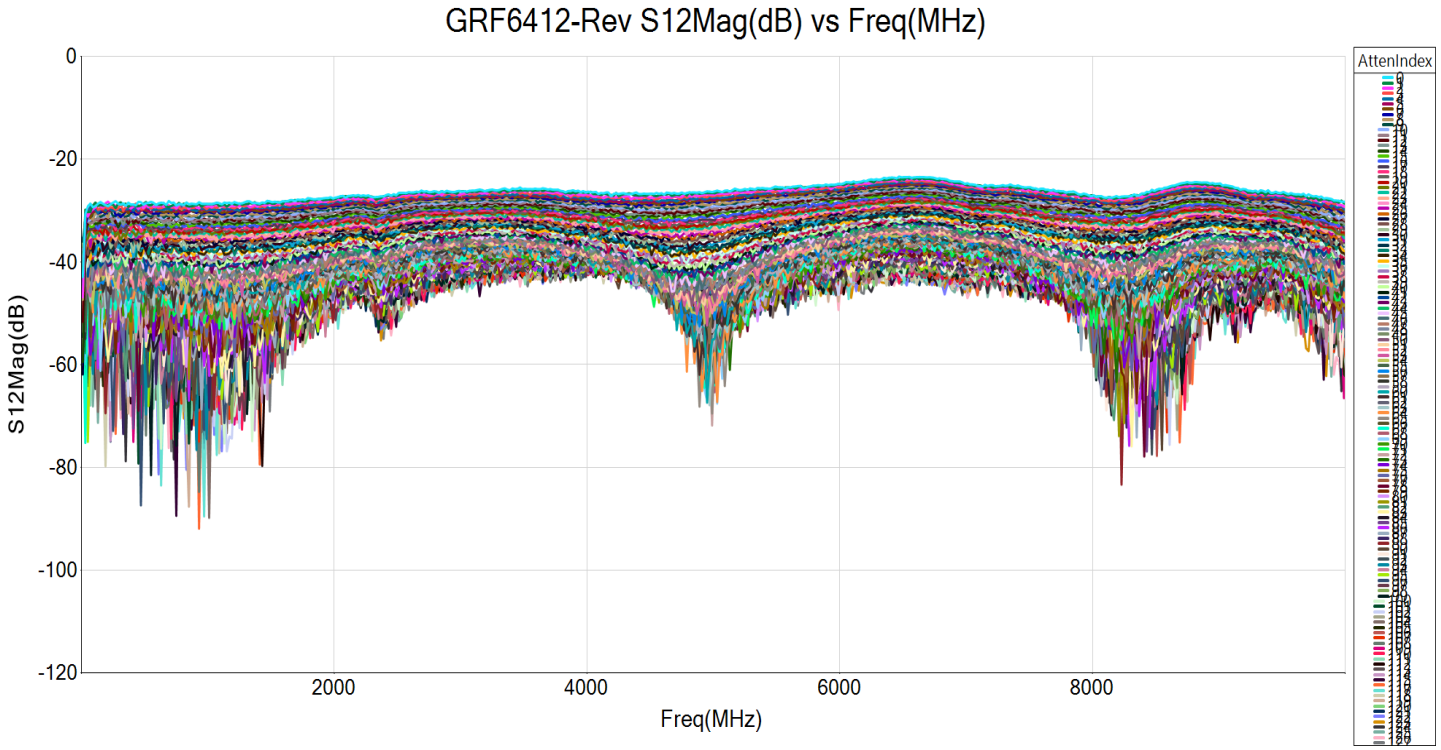


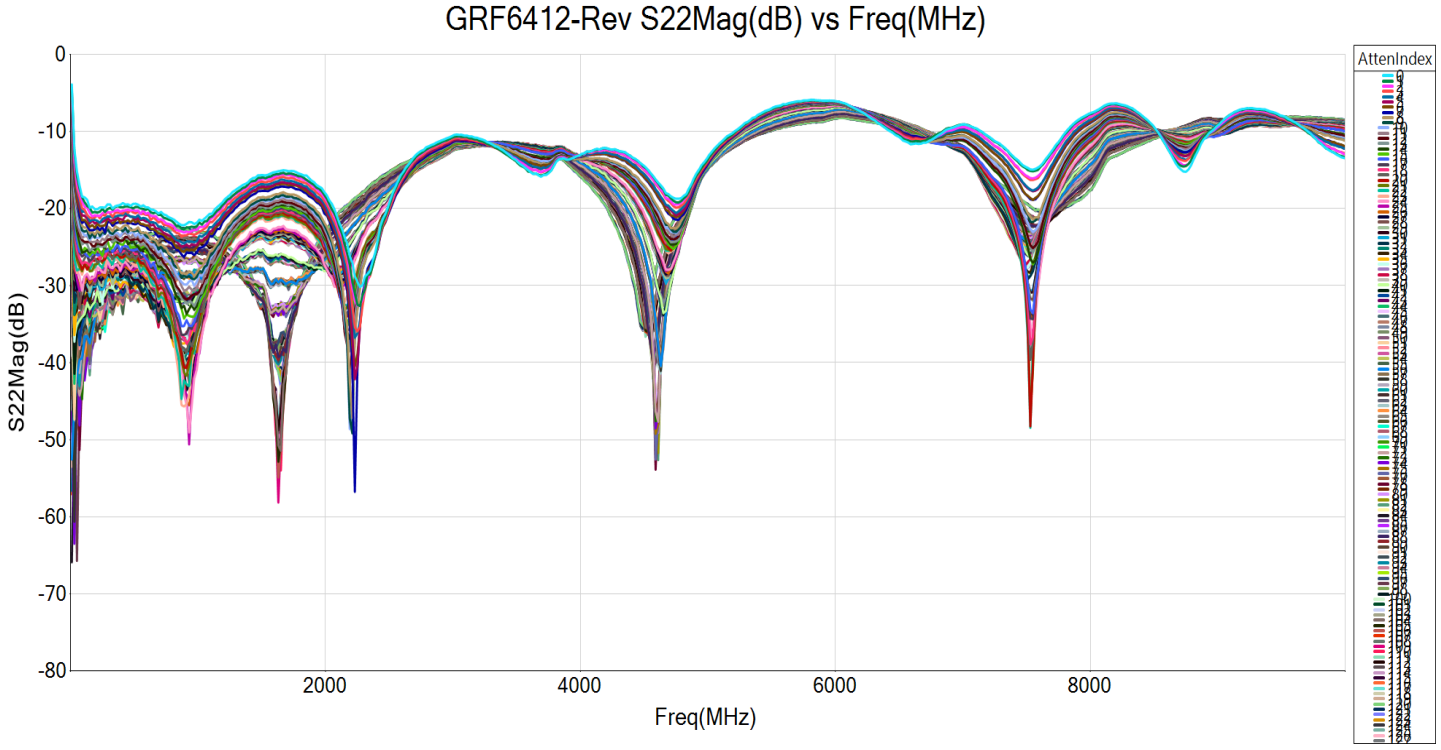
GRF6412 Typical Operating Curves: S-Parameters (AMP to DSA)





GRF6412 Typical Operating Curves: S-Parameters (AMP to DSA)



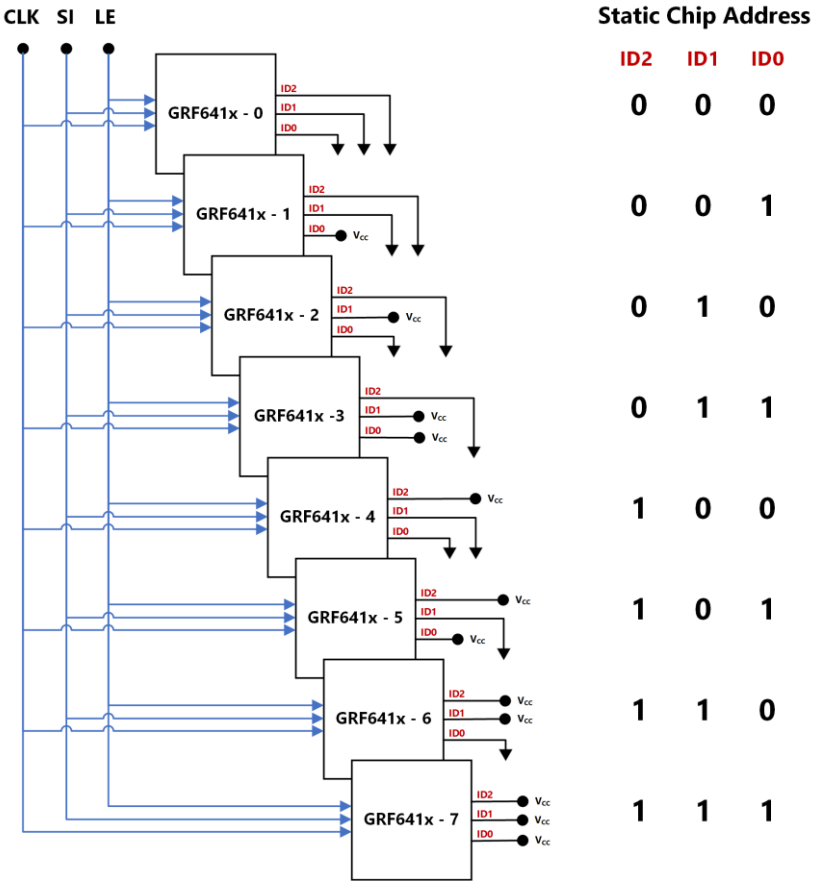


Functional Description

The GRF6412 employs several programming options to control the device's digital step attenuator. The primary programming mode utilizes an enhanced 3-wire SPI (serial-parallel interface) which incorporates multi-device addressing. In addition to supporting traditional serial programming, the GRF6412 also includes a special *Rapid Fire*™ selection pin which allows the device to be immediately switched into a pre-defined attenuation state. The following sections provide specific details on each programming mode.

Multi-IC Addressing Scheme

The GRF6412 has the ability to share a common serial interface line with up to eight similar devices. A unique address is assigned to each component by applying logic to pins ID0 (pin 23), ID1 (pin 13) and ID2 (pin 14). The figure below provides an illustration of such a multi-IC addressing scheme using hardwired logic settings.



Multi-IC Addressing Using Hardwired Logic

As shown, each GRF6412 device shares a common LE control line. The logic present on pins ID0, ID1 and ID2 will be compared with the relevant sub-addressing bits that are delivered as part of the standard 16-bit serial payload. (Refer to the payload figure below for details.) If the addressing in the payload matches the logic on ID0, ID1 and ID2, then the

device recognizes the programming within the payload as being relevant and the SPI commands are executed accordingly. If the addresses do not match, then the device simply ignores the programming command.

Note that utilizing the multi-IC addressing scheme is completely optional. ***If the application only calls for using a single dedicated LE control line, then it is recommended to simply assign a default address of 000 to the device by connecting ID0, ID1 and ID2 to ground.*** The pins can also be floated (i.e. left in a 'no connect' or 'NC' state); if pins ID0, ID1, and ID2 are left floating, the chip address will default to **110** or decimal **6**.

A summary of the chip identifier mapping is provided in the table below:

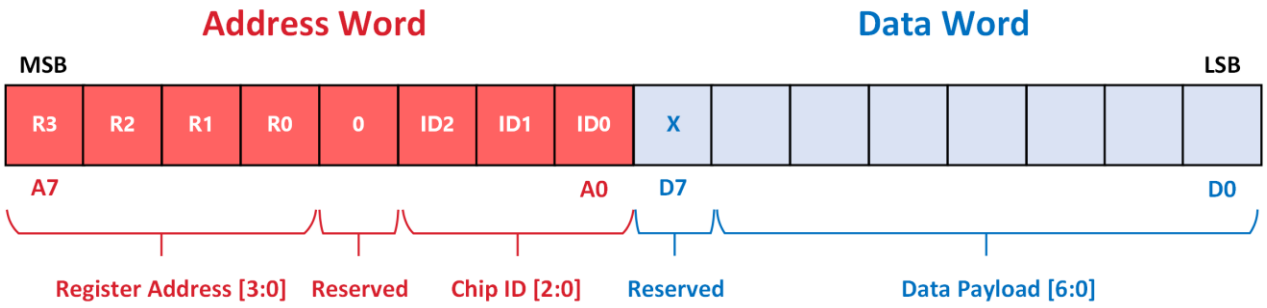
Static Address Truth Table

ID2 (Pin 14)	ID1 (Pin 13)	ID0 (Pin 23)	Static Identifier
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
NC [4]	NC [4]	NC [4]	6
1	1	1	7

Note 4: If left unconnected, ID2 (Pin 14) and ID1 (Pin 13) will default to a logic HIGH state due to internal pull-ups to 1.8V. Conversely, ID0 (Pin 23) will default to a logic LOW state due to an internal pull-down to GND. When all three address pins are left unconnected, the resulting address will be 110 (static identifier '6').

Serial Programming

The GRF6412 utilizes a 16-bit payload to perform its various addressing and programming functions. Information is shifted in with the least significant bit (LSB) first. Refer to the figure below for an overview of the relevant bit assignments:

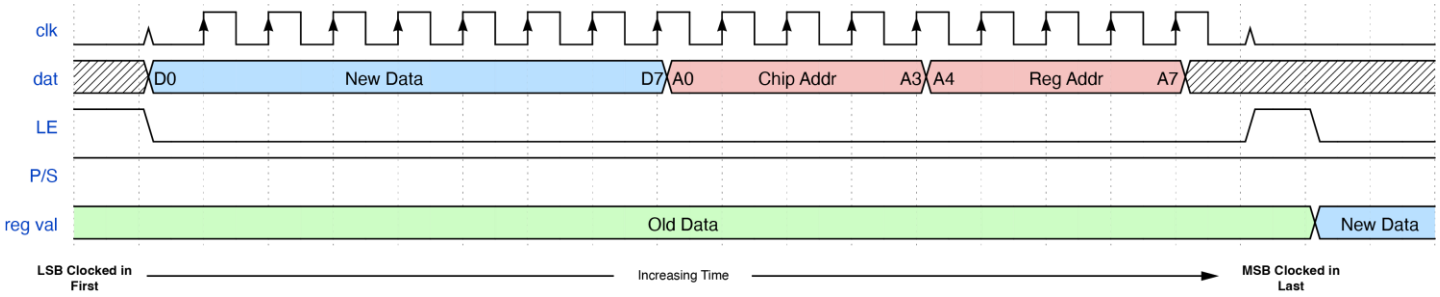


16-Bit SPI Transaction Payload Diagram

The payload consists of two separate 8-bit words. The *data word* is clocked in first. ***Bit D7 is reserved; program in a "0" or a "1" for each SPI transaction***. Bits D6-D0 make up the 7-bit data payload. Note that the data payload will vary depending upon the register being targeted with the write command; *separate 16-bit SPI transactions are therefore required for programming each of the device's three registers.*

The address word is clocked in next. Note that this word includes two separate bit fields. Bits A2-A0 are used to identify the targeted device for each write command, and bits A7-A4 identify the desired register address. ***Bit A3 is reserved, and it must be programmed with a "0" during each SPI transaction.***

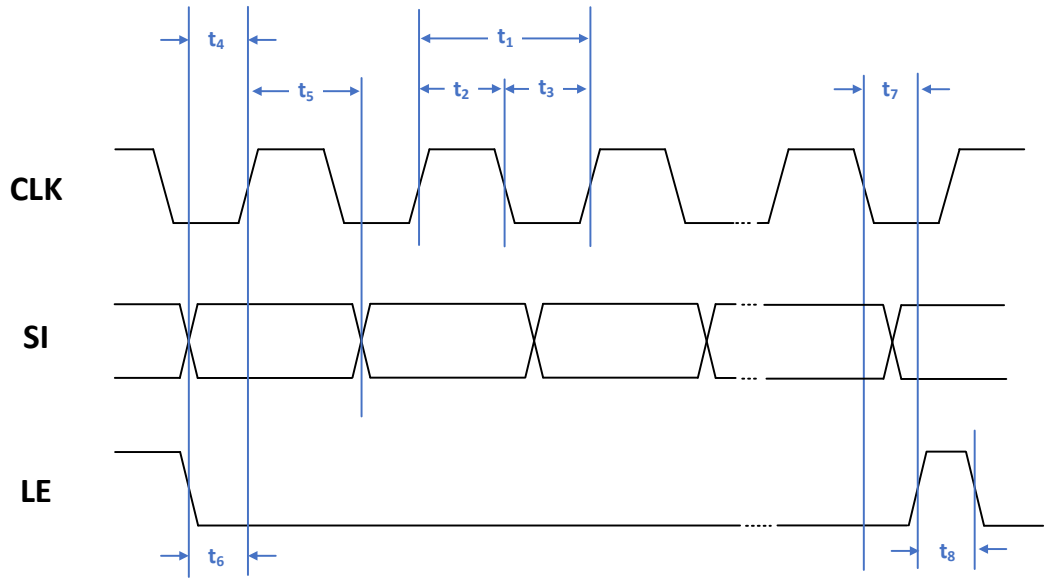
The figure below depicts the timing associated with each programming sequence.



16-Bit SPI Programming Sequence

The sequence begins when the latch enable (LE) line is pulled LOW. After clocking in all 16 bits of the SPI payload, an LE line transition to HIGH will trigger a comparison between bits A3-A0 (the chip ID) with the logic seen on pins ID2, ID1 and ID0. If the two addresses match, then the device will proceed with latching bits D7-D0 into the addressed register. ***This latching process occurs as soon as LE transitions back to LOW.*** If the chip ID bitfield does not match the logic on pins ID2, ID1 and ID0, then the transaction is ignored.

SPI Timing Intervals



SPI Timing Diagram

SPI Timing Specifications

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Serial Clock (CLK) Speed	f_{CLK}			30	MHz	
CLK Period	t_1	33.3			ns	
CLK High Duration Time	t_2	16.7			ns	
CLK Low Duration Time	t_3	16.7			ns	
SI to CLK Setup Time	t_4	10			ns	
SI Hold Time	t_5	10			ns	
LE Low Setup Time	t_6	10			ns	
LE High Setup Time	t_7	10			ns	
LE High Time	t_8	10			ns	

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Register Mapping

The GRF6412 includes 3 separate 8-bit registers which help to facilitate the device's various programming functions. The first register, **ATTEN**, is used to set the device's attenuation state when operated in its normal serial mode. Upon all power-on resets (PORs), the register defaults to [01111111], meaning that the attenuator will be set to its maximum attenuation state.

The **CONFIG** register is used to activate the RFA feature. Upon PORs, all bits within the register will default to 0s, thus placing the RFA feature in a disabled state. If the user decides to employ the RFA option, then the [1] bit field must be set to 1 with a separate SPI transaction. Be sure to leave the [0] bit field set to 0; similarly, bits [7:2] should be set to 0 as well.

The third register, **RFAREG**, is tied to the GRF6412's *Rapid Fire Attenuation* feature. As with the ATTEN register, the RFAREG will default to its maximum attenuation state for all POR conditions. Subsequent SPI programming transactions allow the user to set this register to any customized state between 0 and 31.75 dB. The bit assignments within this particular register get passed along to the attenuator core whenever the RFA feature is enabled ***and*** the external RFA pin (pin 9) goes HIGH.

The remaining registers are unused, and they should NOT be written to with any SPI transactions.

Detailed Register Map

Register Address	Name	Width	Description	Bit Fields	POR Value
0x0	ATTEN	8 bits	Attenuator state when in serial mode.	**[6:0]:** DSA Attenuation Word [1111111] = Max Atten [1000000] = Half Max Atten [0000000] = Min Atten **[7]:** *Unused; must be set to* ***0***	[01111111]
0x1	CONFIG	8 bits	Stores configuration settings	**[0]:** *Rapid Fire Pointer Flag* **0** = RFA attenuation is set from RFAREG **[1]:** *Rapid Fire Feature On/Off Selection* **0** = RFA Disabled **1** = RFA Enabled **[7:2]:** *Unused; all bits must be set to* ***0***	[00000000]
0x2	RFAREG	8 bits	Stores value for Rapid-Fire mode attenuation	**[6:0]:** RFA (Rapid Fire Attenuation) Word [1111111] = Max Atten [1000000] = Half Max Atten [0000000] = Min Atten **[7]:** *Unused; must be set to* ***0***	[01111111]
0x3-0xF	Unused	8 bits	Do not write to these registers		[00000000]

Register Truth Tables

The following truth tables pertain to the attenuator words as used within the ATTEN and RFAREG registers.

7-Bit SPI Word Bit Assignments

Data Bit	Attenuation Control
D7	Not Used
D6	16 dB Attenuator Control
D5	8 dB Attenuator Control
D4	4 dB Attenuator Control
D3	2 dB Attenuator Control
D2	1 dB Attenuator Control
D1	0.5 dB Attenuator Control
D0	0.25 dB Attenuator Control

Serial Control Word Abbreviated Truth Table

Attenuation	D7	D6	D5	D4	D3	D2	D1	D0
0 dB	X	0	0	0	0	0	0	0
0.25 dB	X	0	0	0	0	0	0	1
0.5 dB	X	0	0	0	0	0	1	0
1 dB	X	0	0	0	0	1	0	0
2 dB	X	0	0	0	1	0	0	0
4 dB	X	0	0	1	0	0	0	0
8 dB	X	0	1	0	0	0	0	0
16 dB	X	1	0	0	0	0	0	0
31.75 dB	X	1	1	1	1	1	1	1

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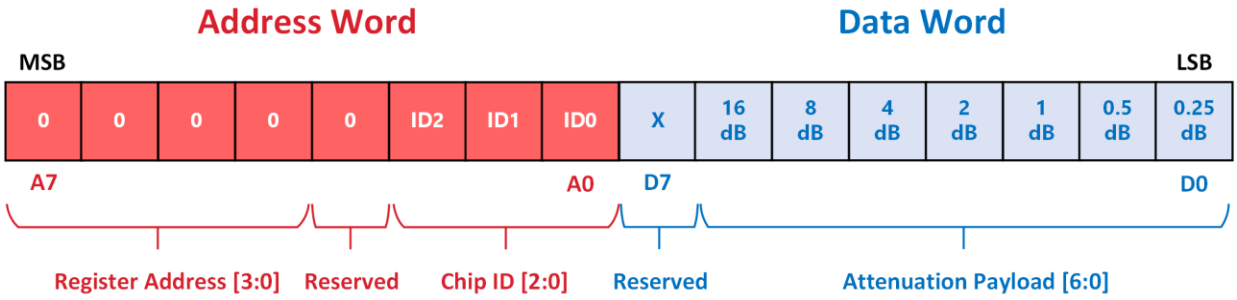
Basic DSA Serial Programming

Upon power-on / reset (POR), the GRF6412 will default to an attenuation setting of 31.75 dB. A simple SPI command can then be executed to change this attenuation setting by writing directly to the device's ATTEN register (0x0). Be sure to include the relevant Chip ID addressing bits, as well as the '0s' noted in the diagram below for bits A3 and D7. Apply the relevant attenuation bits within the data word per the truth tables provided above.

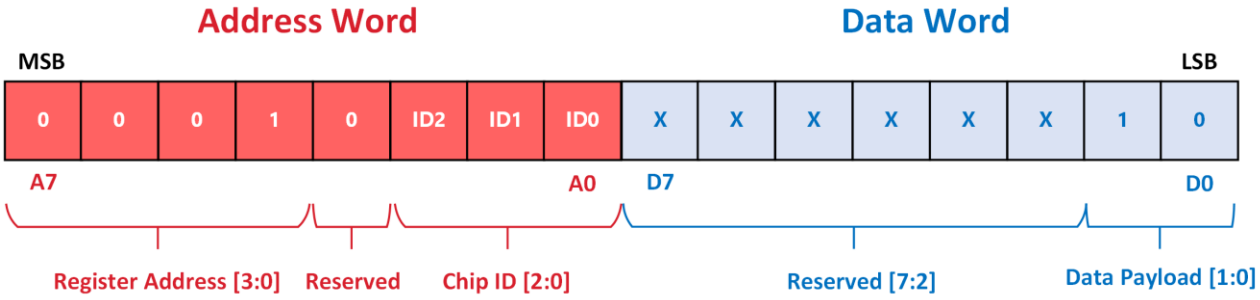


16-Bit SPI Payload for Basic DSA Programming

Rapid Fire™ Attenuation (RFA) Feature

The RFA feature enables the user to quickly switch the attenuator into a pre-defined state, thus circumventing the delays commonly associated with serial programming. A single control line allows the user to rapidly toggle between two attenuation states. In essence, the RFA feature provides a hybrid control mechanism which combines the speed of parallel programming with the convenience of a single control line. This form of control is useful for a multitude of applications where fast switching is critical for protecting downstream stages from overexposure to excessively large RF signals. The ability to quickly shift into a secondary state also allows a single device to be used in TDD applications where different attenuation levels are needed for RX and TX applications.

To use the GRF6412's RFA feature, a one-time SPI command must first be sent to device to activate the feature set. (Note that any subsequent PORs will also require the user to re-activate the RFA feature; PORs force the CONFIG register to revert to its default setting, and the RFA is de-activated as part of this default).

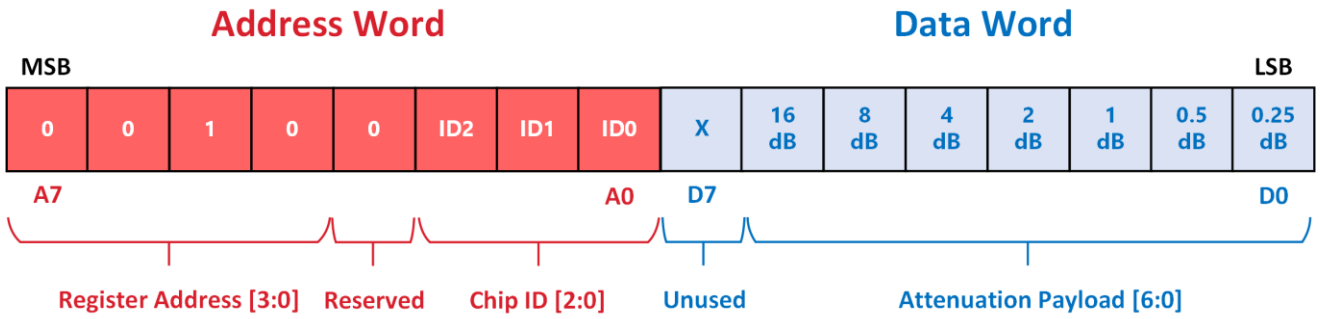


16-Bit SPI Payload for Activating the RFA Feature

Be sure to include the relevant Chip ID addressing bits, as well as the placeholder bits noted in the diagram for bit A3 and D7. D1 is set to "1" to activate the RFA feature. ***Note that D0 must remain as a "0" as part of this activation process.*** (D0 will default to "0" upon PORs). Setting D0 to "0" instructs the device to pull the attenuation setting directly from the RFAREG whenever the RFA pin is pulled HIGH.

To deactivate the RFA feature, simply perform an identical SPI transaction, but set D1 to "0" instead.

To customize the amount of attenuation being 'fired in', an additional SPI command must also be sent to change the RFA level from its default of 31.75 dB. Simply perform a separate SPI transaction to write to the RFAREG:



16-Bit SPI Payload for Customizing the RFA's Attenuation Setting

As mentioned earlier, be sure to include the relevant Chip ID addressing bits, as well as the placeholder bits noted in the diagram for bits A3 and D7. Apply the relevant attenuation bits within the data word per the truth tables provided above.

Using the GRF640X/GRF641X DSA Control GUI

Requirements

Windows PC with the following:

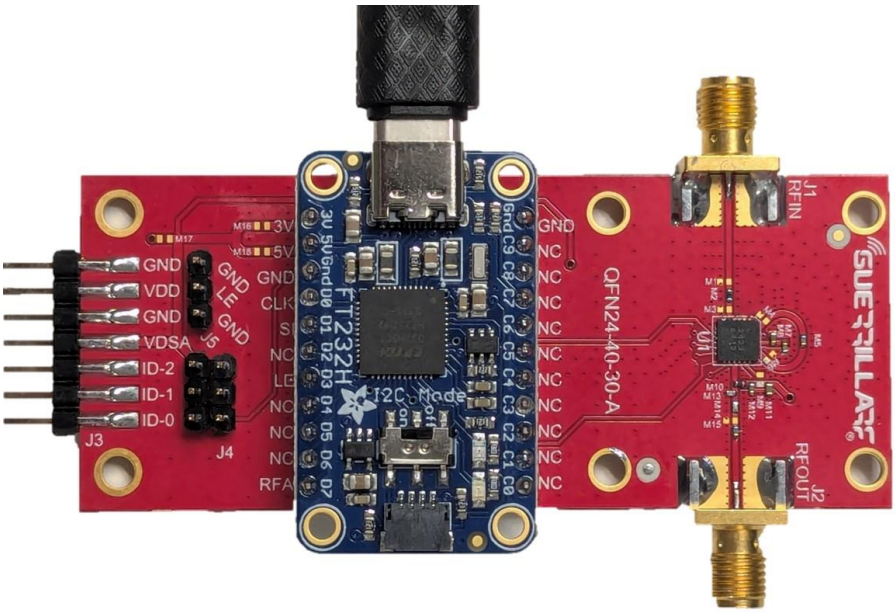
- Windows 10 (or newer) operating system. (Note: the GUI will not run on Mac OS or Linux machines.)
- USB-C capability (either native or via a USB-A to USB-C adapter)

GRF Control GUI

- Executable GUI Application File (.exe)
- GUI can be downloaded directly from the GRF6412 product page. Click here to access the page within Guerrilla RF's website.

Overview

The GRF6412 evaluation board is designed to work in conjunction with the *Adafruit FT232H USB-C to GPIO, SPI, and I2C Controller*. This separate breakout board attaches directly to the GRF6412's QFN24-40-30-C evaluation board as shown below. After downloading the GRF DSA control software, any USB-C equipped PC running Windows 10 (or newer) can be used to activate the control panel GUI. Please note that more in-depth programming details can be found in the "Detailed Register Map" section of this data sheet.



The evaluation board is connected to a USB-C equipped Adafruit breakout board

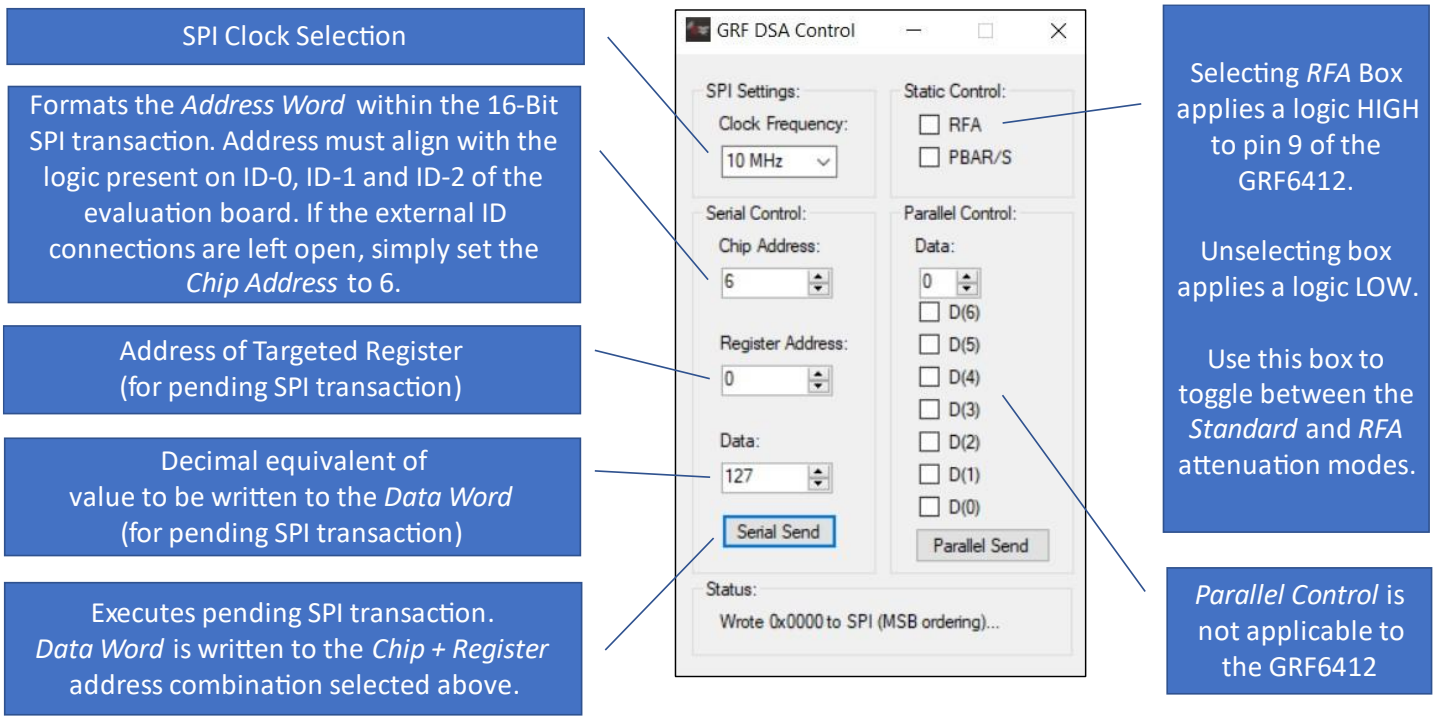
Getting Started

After downloading the GUI control application onto your PC, simply follow the steps below to initiate communication between your PC and the GRF6412 evaluation board.

1. Connect the Adafruit controller to your computer via any USB-C connection. The appropriate drivers for the controller should load automatically for PCs running Windows 10 or 11.
2. To activate the "GRF DSA Control" GUI, launch the executable called "grf_dsa_gui.exe."

Note: Since the GUI is an executable file, your PC's security software may prevent you from simply downloading and running the application without some form of override or intervention. Review the instructions associated with your preferred security software to allow the executable to launch.

Once launched, the GUI application will reveal the control panel shown below.



The DSA Control Panel

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Selectable Control Options

SPI SETTINGS

Clock Frequency

- Use the pull-down menu to select from a set of pre-determined frequencies ranging from 1 MHz to 30 MHz.

SERIAL CONTROL

Chip Address

- This entry automatically formats the three address bits (A0-A2) used within the 16-bit SPI transaction.
- Select from *one of the 8* possible addresses supported by the GRF6412.
- The selected address must align with the logic being assigned to the ID-0, ID-1, and ID-2 control pins on the evaluation board's J3 header.
- If external logic is not provided via the J3 header, then the GRF6412 will have a default address of "**6**" [As noted in the data sheet's "Static Address Truth Table," internal pull-ups/pull-downs on the device's three address pins (A0-A3) will force the address logic on these pins to state 110 (i.e. address 6) when the pins are left unconnected.]

Register Address

- This entry selects the targeted register to be written to with the pending SPI transaction.
- Select from one of 3 possible addresses.
    - Address 0: ATTEN register
    - Address 1: CONFIG register
    - Address 2: RFAREG register

Data

- Use this entry to program bits D0-D7 (the data word) for the pending SPI transaction.
- Select from one of 128 possible word combinations.
    - 0 = x0000000
    - 127 = x1111111

Serial Send

- Click on the "Serial Send" button when ready to execute the SPI transaction.
- All data present within the "Chip Address," "Register Address" and "Data" fields will be formatted and sent to the GRF6412 via a 16-bit word.

STATIC CONTROL

- Use the "Static Control" boxes to select the logic on the RFA (applicable for the GRF6412) and PBAR/S (applicable for the GRF6403) pins.
- Note: *Rapid Fire* feature must be first enabled within the CONFIG register in order for the RFA functionality to respond to these commands.
- RFA Logic Assignments *(**GRF6412 Only**)*
    - RFA box checked: Logic HIGH assigned to pin 9 [RFA attenuation (from Register 2) Switched In]
    - RFA box unchecked: Logic LOW assigned to pin 9 [Primary Attenuation (from Register 0) Switched In]
- PBAR/S Logic Assignments *(**GRF6403 Only**)*
    - This static control box is only applicable to the GRF6403; selecting/unselecting the box has no impact on the GRF6412
    - PBARS/S box checked: Logic HIGH assigned to pin 3 on the GRF6403
    - PBARS/S box unchecked: Logic LOW assigned to pin 3 on the GRF6403

PARALLEL CONTROL (Applicable to the *GRF6403 Only*)

Data

- Use this entry to program in the external logic for bits D0-D6 (pins 1, 24, 23, 22, 21, 20 and 19) on the GRF6403
- Select from one of 128 possible word combinations.
    - 0 = x0000000
    - 127 = x1111111

Parallel Send

- Click on the "Parallel Send" button when ready to apply the parallel logic to pins 1, 24, 23, 22, 21, 20 and 19 on the GRF6403

Changing the Attenuation Level within the ATTEN Register

1. To make any changes via the GUI, be sure that the "Chip Address" matches up with the logic being applied to the ID-0, ID-1 and ID-2 connections on the evaluation board. If these connections have been left "Open," then be sure to set the chip address to "6."
2. Set the "Register Address" to "0" to select the "ATTEN" register.
3. Select the desired attenuation step within the data field. Since the GRF641x series are 7-bit devices, there are 128 discrete 0.25 dB steps. Selecting a "0" in the data field places the DSA in its MINIMUM attenuation state. Conversely, selecting 127 will activate all of the attenuation cells, resulting in a MAXIMUM attenuation state of 31.75 dB. Use the following equation to select the desired attenuation state:

$$\text{ATTEN State (decimal)} = [\ \text{ATTEN State (dB)}\ ] / 0.25$$

4. The "Static Control" and "Parallel Control" fields can be ignored when simply programming the primary ATTEN DSA register.
5. Click on the "Serial Send" button to execute the SPI transaction. Assuming the RFA bit is set to "0" (i.e. the RFA static control box is left unchecked), the DSA will load in the new attenuation value as soon as the SPI transaction is completed.

Utilizing the *Rapid Fire*™ Feature Via the GUI

The control panel can be used to switch between the two attenuation states (standard and *Rapid Fire*™) by simply using the RFA checkbox in the "Static Control" field. However, in order to use the RFA feature, the *Rapid Fire*™ option must first be activated within the CONFIG register.

Enabling the *Rapid Fire*™ Feature on the GRF6412

1. Make sure that the "Chip Address" entry is set to the proper address per the instructions above.
2. Set the "Register Address" to 1 to select the CONFIG register.
3. Set the "Data" field to 2.
4. Hit the "Serial Send" button. Doing so will write a "10" to data bits D0-D1 within the CONFIG register.

Setting the *Rapid Fire*™ Attenuation State

Upon PORs (Power on Resets), the RFAREG (*Rapid Fire* register) will automatically be set to represent a full attenuation state of 31.75 dB. To override this default attenuation state, simply reprogram the values in RFAREG with the followings steps:

1. Make sure that the "Chip Address" entry is set to the proper address per the instructions above.
2. Set the "Register Address" to 2 to select the RFAREG register.
3. Select the desired attenuation step within the data field. As with the ATTEN register, there are 128 discrete 0.25 dB steps that can be chosen. Selecting a "0" in the data field places the DSA in its MINIMUM attenuation state. Conversely, selecting 127 will activate all of the attenuation cells, resulting in a MAXIMUM attenuation state of 31.75 dB. Use the following equation to select the desired attenuation state:

   RFA ATTEN state (decimal) = [RFA ATTEN State (dB)] / 0.25

4. Hit the "Serial Send" button.

Toggling Between the Standard and *Rapid Fire*™ Attenuation States

Once the *Rapid Fire*™ feature has been enabled within the CONFIG register, simply apply a checkmark to the RFA box within the Static Control Field.

- RFA box checked: Logic HIGH assigned to pin 9 [RFA Attenuation (from Register 2) Switched In]
- RFA box unchecked: Logic LOW assigned to pin 9 [Primary Attenuation (from Register 0) Switched In]

Please note that more in-depth programming details can be found in the "Detailed Register Map" section of this data sheet.

RF Configurations

As noted within the *Pin Description* section, the RF ports of the DSA and AMP cores are fully accesssible via external pinning. The two cores are completely independent, and they can be configured in a variety of ways within different RF lineups.

DSA Core

The DSA is a fully reciprocal device; as such, each RF port (DSA_1 or DSA_2) can be used as an input or output. This reciprocity allows the DSA to be placed before or after the AMP stage as shown in the application circuits below.

The DSA_1 and DSA_2 ports are internally matched to 50 Ω, so no external matching is required. However, ***DC blocking capacitors must be used if there is voltage present on the RF lines from the preceding or following stages.*** As a matter of good practice, it is recommended that DC blocks be used as a precaution.

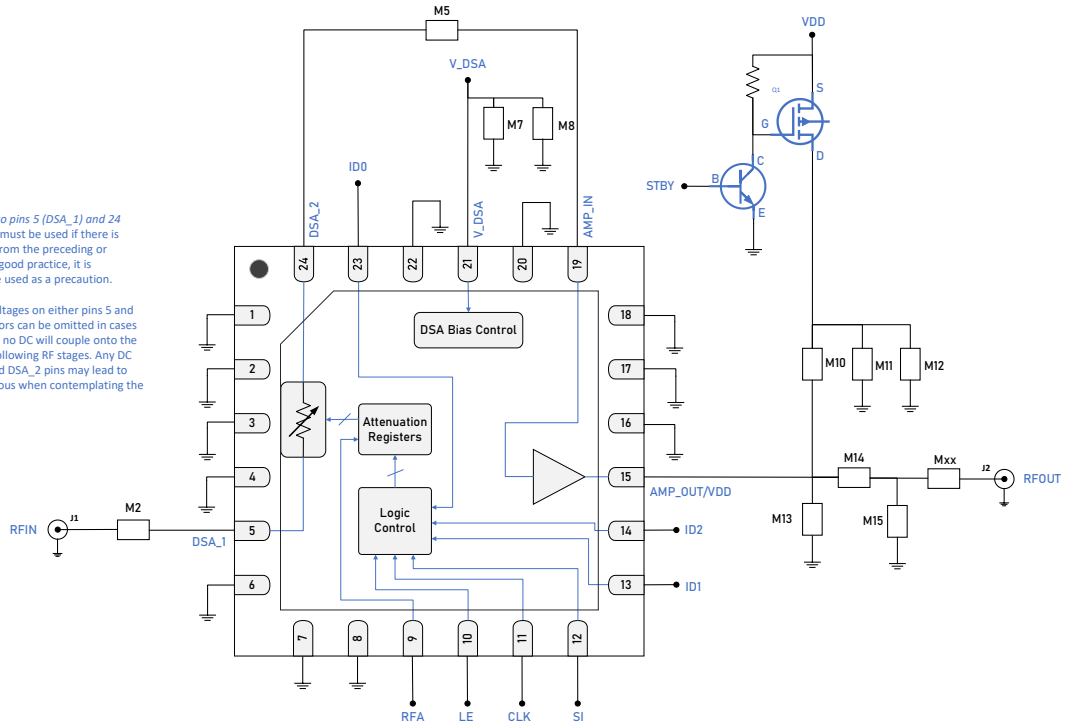
Note that the DSA will not generate DC voltages on either pins 7 and 14, so the blocking capacitors can be omitted in cases where it can be guaranteed that no DC will couple onto the RF lines from the preceding or following RF stages. Any DC voltage applied to the DSA_1 and DSA_2 pins may lead to electrical overstress, so be cautious when contemplating the removal of these components.

AMP Core

The amplifier core is a broadband, highly linear gain block that is intended to be used within 50 Ω systems. The amplifier's input port typically requires a one- or two-element series-shunt match, while the output port requires a three-element match. DC bias for the core is fed in to the AMP_OUT port via an RF choke. To place the amplifier in standby (STBY) mode, consider implementing a simple supply rail switch as shown below. Refer to the following application drawings for recommended component placement and value selection. As with most of Guerrilla RF's amplifier cores, additional tuning options can be found on the device's product page under the 'Custom Tunes' tab. Contact Guerrilla RF's applications team at applications@guerrilla-rf.com for additional assistance.

NOTE: *Do not apply DC voltage to pins 5 (DSA_1) and 24 (DSA_2).* DC blocking capacitors must be used if there is voltage present on the RF lines from the preceding or following stages. As a matter of good practice, it is recommended that DC blocks be used as a precaution.

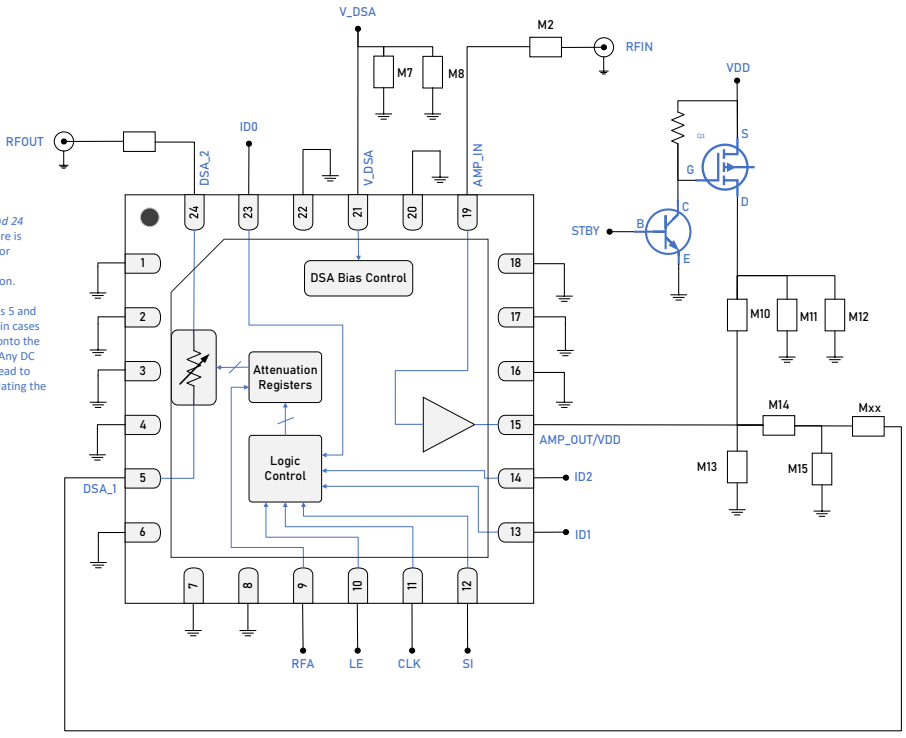
The DSA will not generate DC voltages on either pins 5 and 24; as such, the blocking capacitors can be omitted in cases where it can be *guaranteed* that no DC will couple onto the RF lines from the preceding or following RF stages. Any DC voltage applied to the DSA_1 and DSA_2 pins may lead to electrical overstress, so be cautious when contemplating the removal of these components.



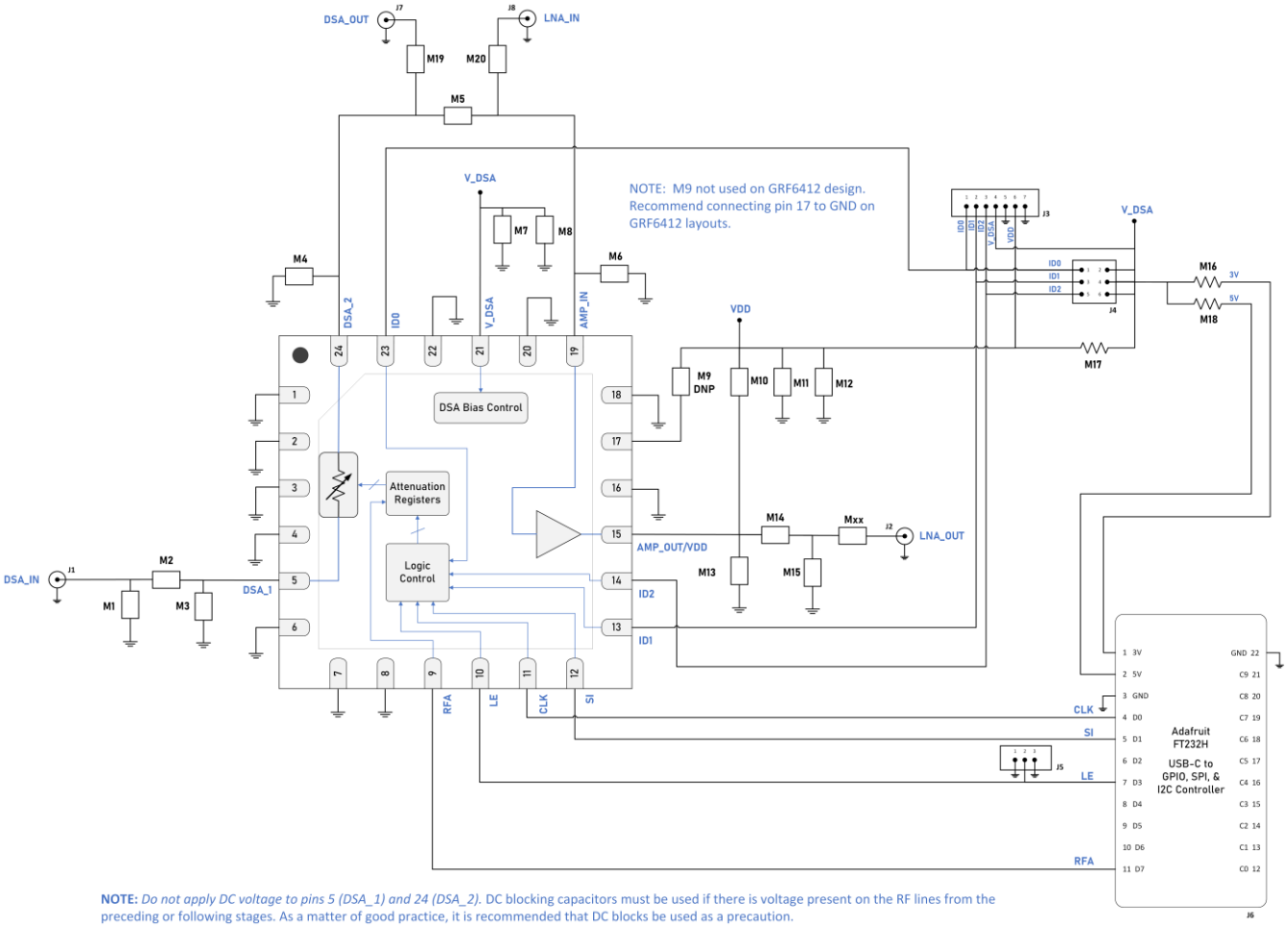
GRF6412 Applications Circuit: DSA → Amplifier Cascade with External Supply Rail Switch

NOTE: *Do not apply DC voltage to pins 5 (DSA_1) and 24 (DSA_2).* DC blocking capacitors must be used if there is voltage present on the RF lines from the preceding or following stages. As a matter of good practice, it is recommended that DC blocks be used as a precaution.

The DSA will not generate DC voltages on either pins 5 and 24; as such, the blocking capacitors can be omitted in cases where it can be *guaranteed* that no DC will couple onto the RF lines from the preceding or following RF stages. Any DC voltage applied to the DSA_1 and DSA_2 pins may lead to electrical overstress, so be cautious when contemplating the removal of these components.



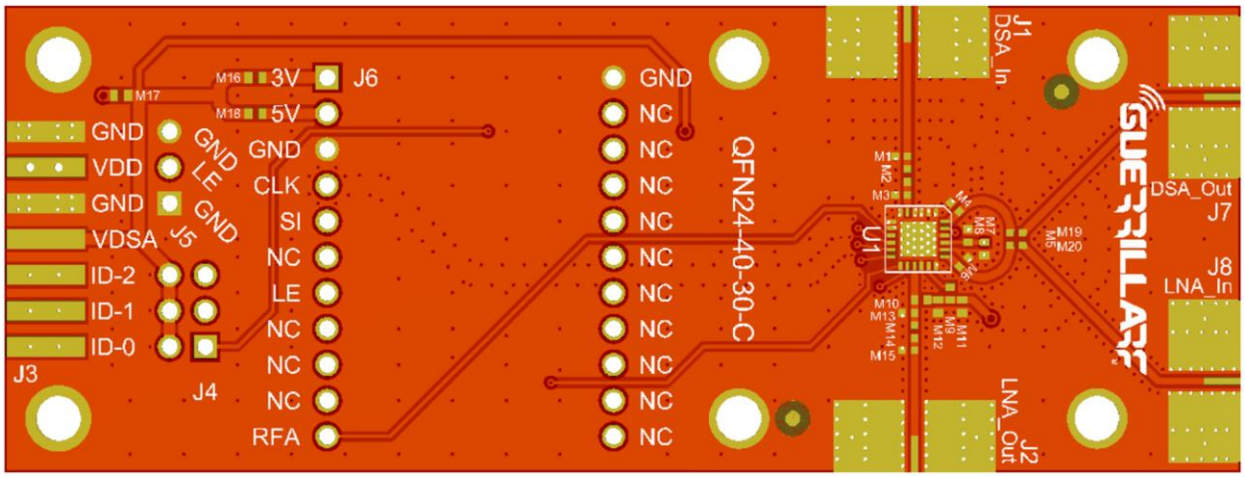
GRF6412 Applications Circuit: Amplifier → DSA Cascade with External Supply Rail Switch



NOTE: *Do not apply DC voltage to pins 5 (DSA_1) and 24 (DSA_2).* DC blocking capacitors must be used if there is voltage present on the RF lines from the preceding or following stages. As a matter of good practice, it is recommended that DC blocks be used as a precaution.

The DSA will not generate DC voltages on either pins 5 and 24; as such, the blocking capacitors can be omitted in cases where it can be *guaranteed* that no DC will couple onto the RF lines from the preceding or following RF stages. Any DC voltage applied to the DSA_1 and DSA_2 pins may lead to electrical overstress, so be cautious when contemplating the removal of these components.

GRF6412 Evaluation Board Schematic



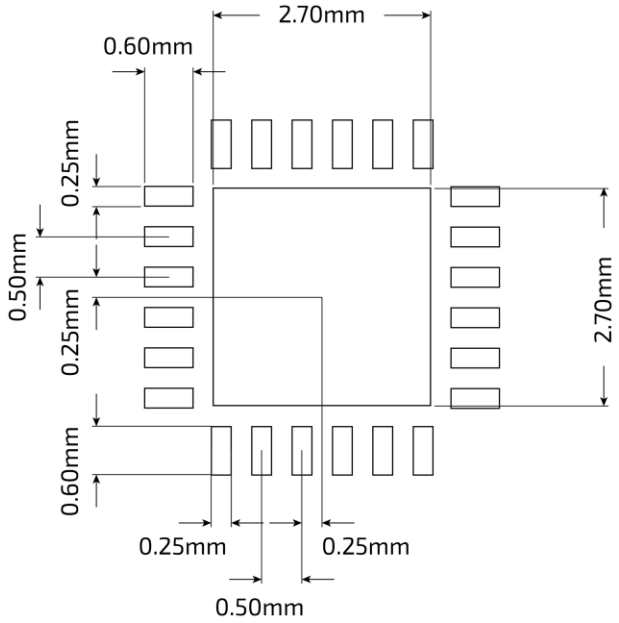
GRF6412 Evaluation Board Assembly Diagram

GRF6412 Evaluation Board Assembly Diagram Reference

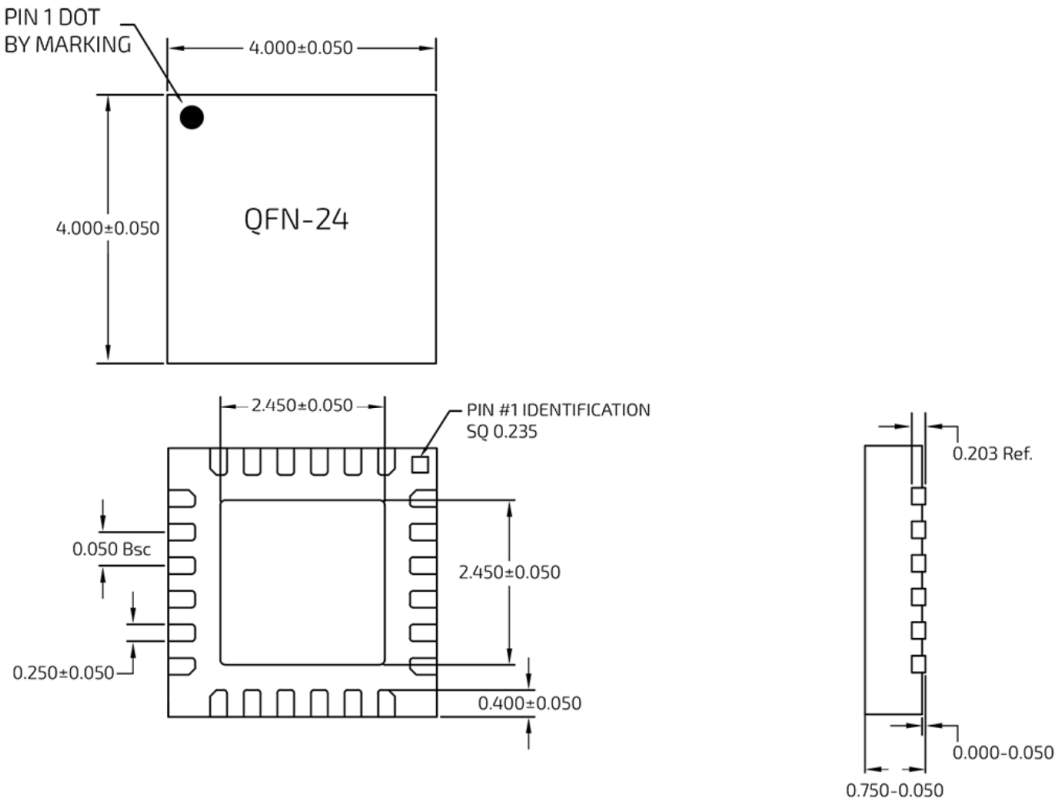
Component	Type	Manufacturer	Family	Value	Package Size	Substitution
M1				DNP		Ok
M2	Resistor	Murata	--	0 Ω	0201	Ok
M3				DNP		Ok
M4				DNP		Ok
M5	Capacitor	Murata	GRM	1000 pF	0201	Ok
M6				DNP		Ok
M7	Capacitor	Murata	GJM	10 nF	0201	Ok
M8	Capacitor	Murata	GJM	1 µF	0402	Ok
M9				DNP		
M10	Ferrite Bead	Murata	BLM15HG102BH1	1 kΩ	0402	Ok
M11	Capacitor	Murata	GJM	10 µF	0402	Ok
M12	Capacitor	Murata	GRM	1000 pF	0402	Ok
M13	Capacitor	Murata	GJM	0.3 pF	0201	Ok
M14	Resistor	Murata	--	0 Ω	0201	Ok
M15				DNP		
M16				DNP		
M17	Resistor	Murata	--	0 Ω	0201	Ok
M18	Resistor	Murata	--	0 Ω	0201	Ok
M19				DNP		
M20				DNP		
Mxx	Capacitor	Murata	GJM	1000 pF	0201	Ok
Control Board	FT232H USB-C to GPIO, SPI and I2C Controller	Adafruit **(note 6)**				
Evaluation Board	QFN24-40-30-C					

Note 5: Standard evaluation board bias: V_{DD} = 5 V, V_{DSA} = 5 V.

Note 6: For additional product details, go to https://www.adafruit.com/product/2264 .



4 x 4 mm QFN-16 Suggested PCB Footprint (Top View)



4 x 4 mm QFN-24 Package Dimensions

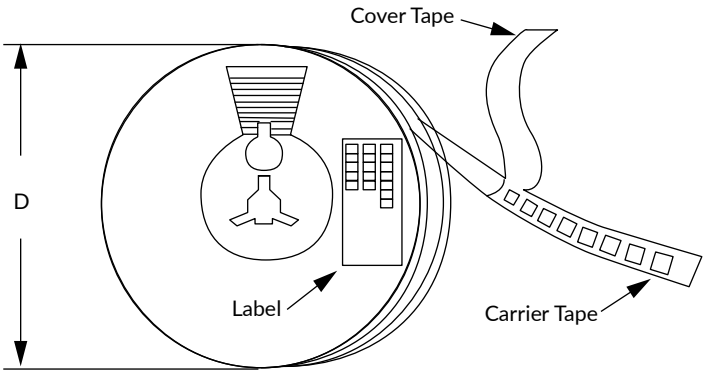
Package Marking Diagram

- Line 1: "YY" = YEAR and "WW" = WEEK the device was assembled.
- Line 2: "GRF" = GUERRILLA RF.
- Line 3: "XXXX" = PART NUMBER.

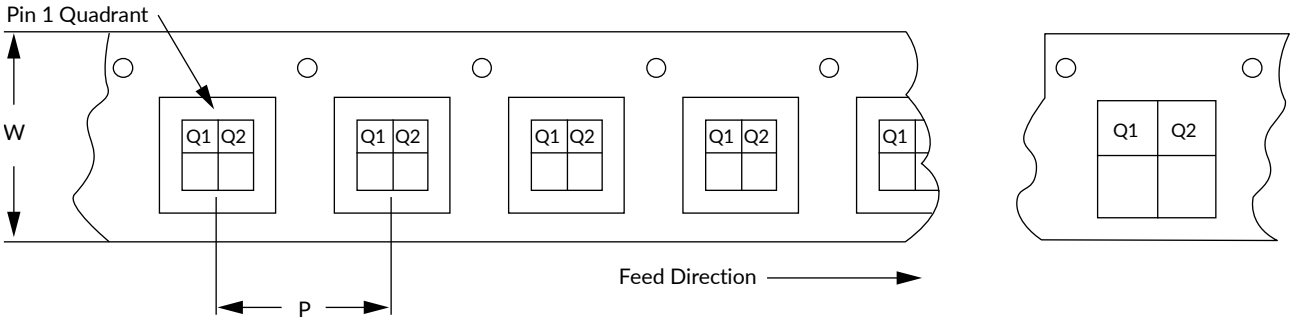
Tape and Reel Information

Guerrilla RF's tape and reel specification complies with Electronic Industries Alliance (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). See the following page for the Tape and Reel Specification and Device Package Information table, which includes units per reel.

Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag and the outside surface of the box.



Tape and Reel Packaging with Reel Diameter Noted (D)



Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information

Revision History

Revision Date	Description of Change
February 10, 2025	Advance Data Sheet – Initial Draft.
February 19, 2025	Extended max frequency rating from 6 GHz to 8 GHz. Modified EVB drawings to enable DSA → AMP and AMP → DSA configurations. Updated package drawings to reflect 4x4 mm QFN-24 packaging.
March 4, 2025	Preliminary Data Sheet. Replaced IC image on page 1. Added suggested PCB footprint drawing. Added S-Parameter plots.

Data Sheet Classifications

Data Sheet Status	Notes
Advance	S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices.
Preliminary	All data based on limited evaluation board measurements taken within the Guerrilla RF Applications Lab. All parametric values are subject to change pending the collection of additional data.
Release Ø	All data based on measurements taken with *production-released* material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory.
Release A-Z	All data based on measurements taken with production-released material *derived from multiple lots which have been fabricated over an extended period of time*. MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads.