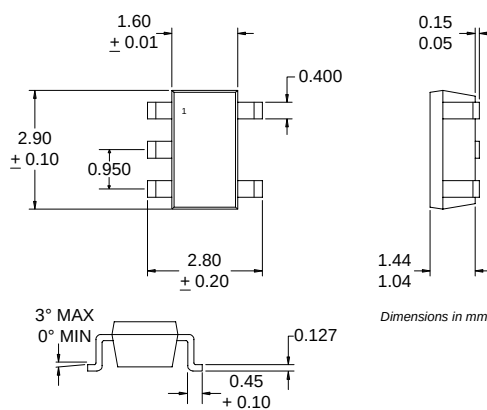


Typical Applications

- Broadband Gain Blocks
- Final PA for Low-Power Applications
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Oscillator Loop Amplifiers

Product Description

The RF2325 is a general purpose, low-cost silicon amplifier designed for operation from a 3V supply. The Darlington circuit configuration with resistive feedback allows for broadband cascadable amplification. The device is unconditionally stable and internally matched to 50Ω. The only external components required for specified performance are bypass and DC blocking capacitors and two bias elements (as shown in application schematic). The RF2325 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



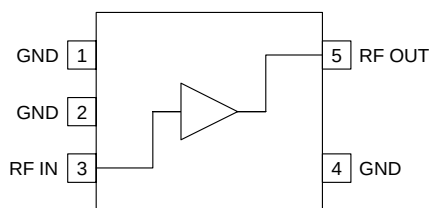
Optimum Technology Matching® Applied

- | | | |
|--|-----------------------------------|--------------------------------------|
| ☒ Si BJT | ☐ GaAs HBT | ☐ GaAs MESFET |
| ☐ Si Bi-CMOS | ☐ SiGe HBT | ☐ Si CMOS |

Package Style: SOT 5-Lead

Features

- DC to >2000MHz Operation
- 2.7V to 3.3V Single Supply
- +17dBm Output IP3
- 16dB Gain at 900MHz
- 12dB Gain at 1900MHz
- Internally 50Ω Matched Input and Output



Functional Block Diagram

Ordering Information

RF2325	3V General Purpose Amplifier
RF2325 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
Fax (336) 664 0454
<http://www.rfmd.com>

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	4.0	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-55 to +150	°C



Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

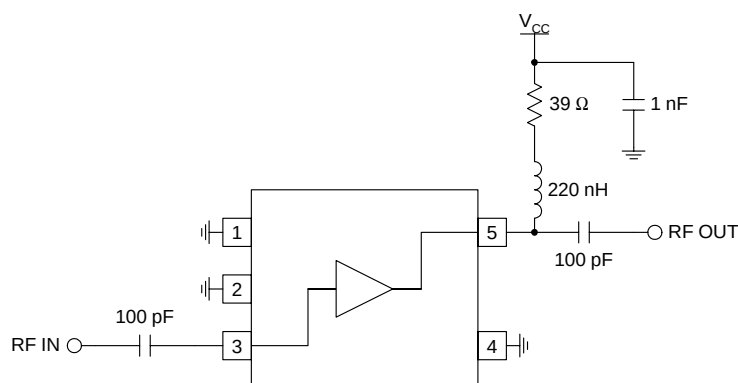
4

GENERAL PURPOSE
AMPLIFIERS

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=27 °C, V _{CC} =3.0V
Frequency Range		DC to >2000		MHz	
100MHz Performance					T=27 °C, V _{CC} =3.0V
Gain		20		dB	
Noise Figure		5.0		dB	
Output IP3		18		dBm	
Output P _{1dB}		8		dBm	
Input Return Loss		15		dB	
Output Return Loss		18		dB	
Isolation		23		dB	
500MHz Performance					T=27 °C, V _{CC} =3.0V
Gain		19		dB	
Noise Figure		5.0		dB	
Output IP3		18		dBm	
Output P _{1dB}		7		dBm	
Input Return Loss		12		dB	
Output Return Loss		23		dB	
Isolation		22		dB	
900MHz Performance	15.3	16	17.3		T=27 °C, V _{CC} =3.0V
Gain		16		dB	
Noise Figure		5.0		dB	
Output IP3		17		dBm	
Output P _{1dB}		7		dBm	
Input Return Loss		10		dB	
Output Return Loss		20		dB	
Isolation		22		dB	
1000MHz Performance					T=27 °C, V _{CC} =3.0V
Gain		16		dB	
Noise Figure		5.0		dB	
Output IP3		17		dBm	
Output P _{1dB}		7		dBm	
Input Return Loss		10		dB	
Output Return Loss		19		dB	
Isolation		22		dB	
2000MHz Performance					T=27 °C, V _{CC} =3.0V
Gain		12		dB	
Noise Figure		5.4		dB	
Output IP3		16		dBm	
Output P _{1dB}		6		dBm	
Input Return Loss		10		dB	
Output Return Loss		17		dB	
Isolation		19		dB	
Power Supply					
Operating Voltage		3.0±10%		V	
Operating Current	23.5	27	29.5	mA	V _{CC} =3.0V

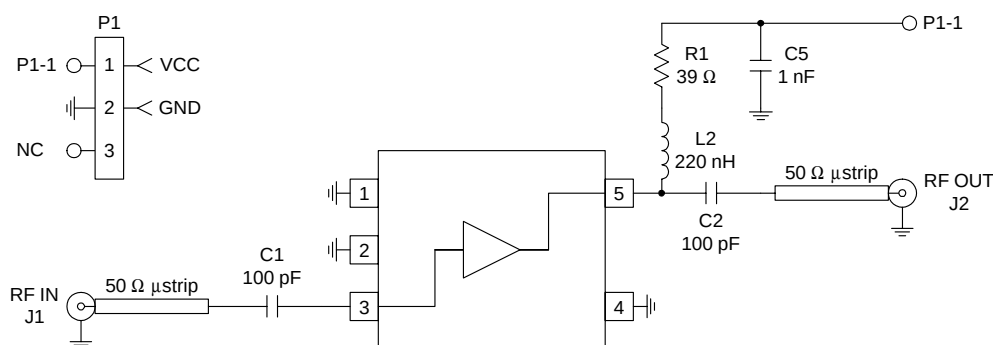
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	RF IN	RF input pin. This pin is not externally DC blocked and thus requires an external blocking capacitor suitable for the frequency of operation. The input impedance of this pin is internally matched to 50Ω using resistive feedback.	
4	GND	Same as pin 1.	
5	RF OUT	RF output and bias pin. The input impedance of this pin is internally matched to 50Ω using resistive feedback. Bias should be supplied to this pin through an external series resistor and RF choke inductor. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well-bypassed.	See pin 3 schematic.

Application Schematic

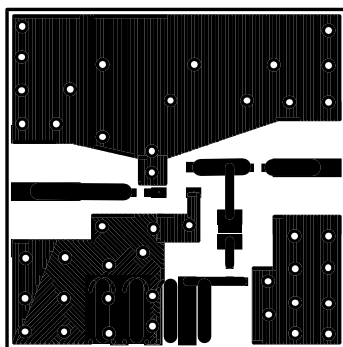
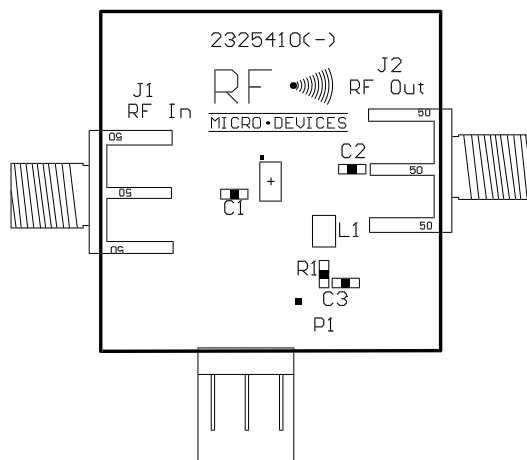


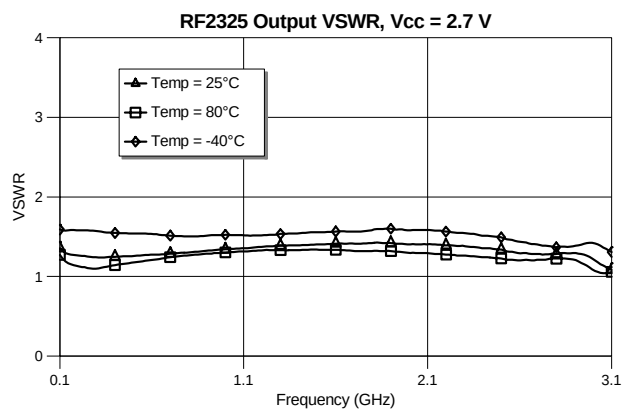
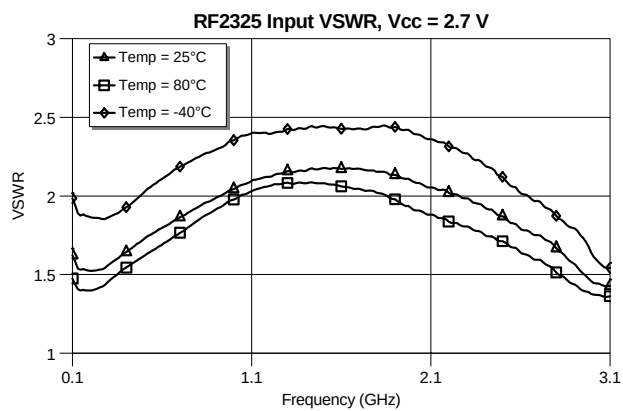
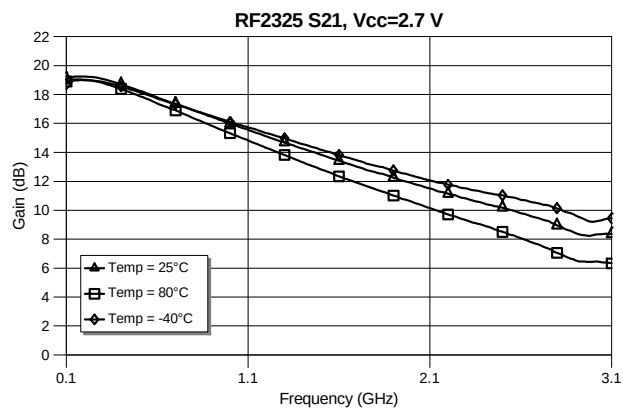
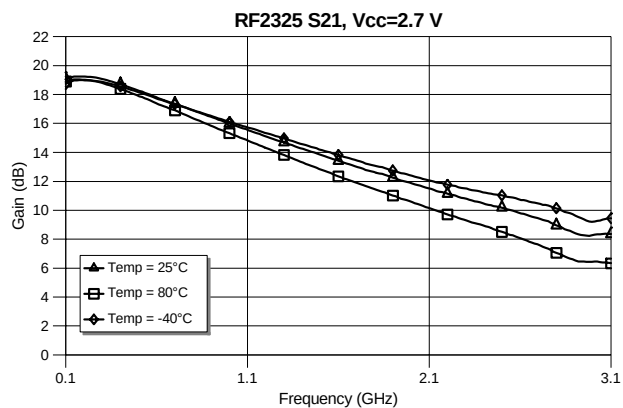
Evaluation Board Schematic

(Download [Bill of Materials](http://www.rfmd.com) from www.rfmd.com.)

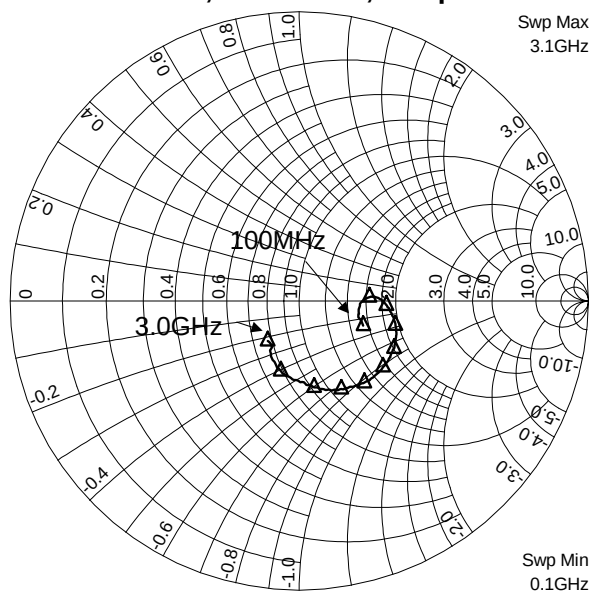


Evaluation Board Layout 1" x 1"

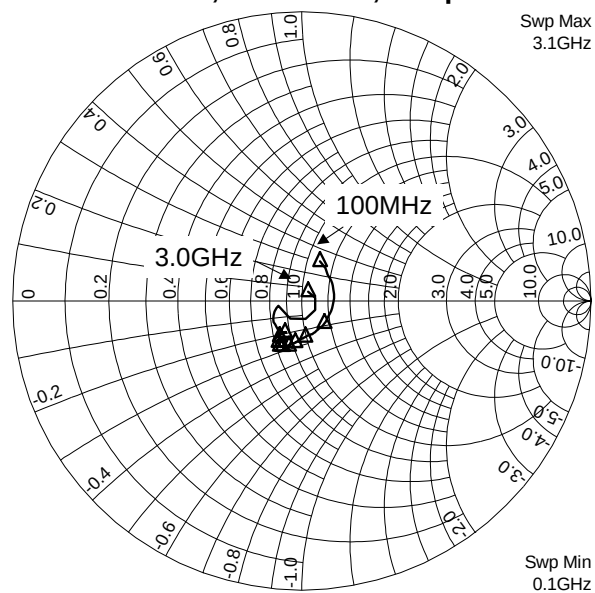


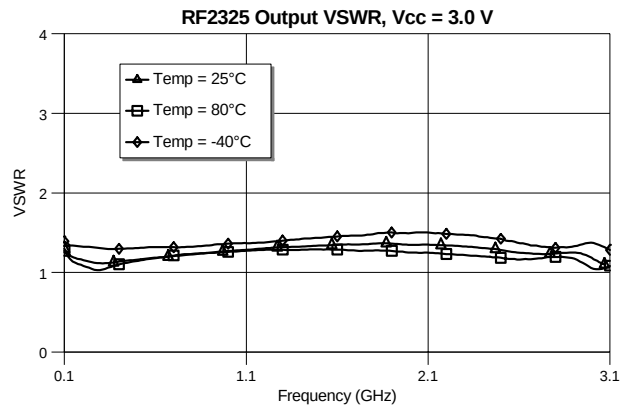
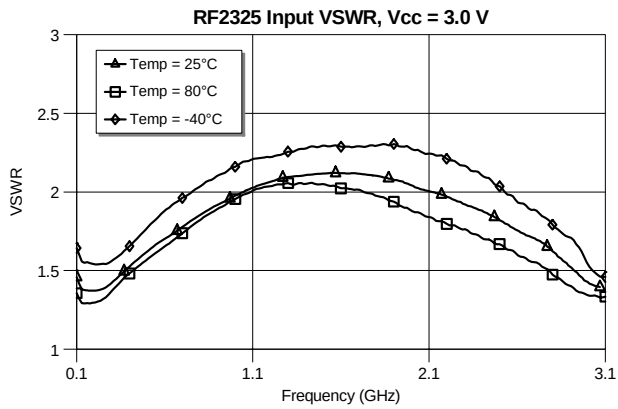
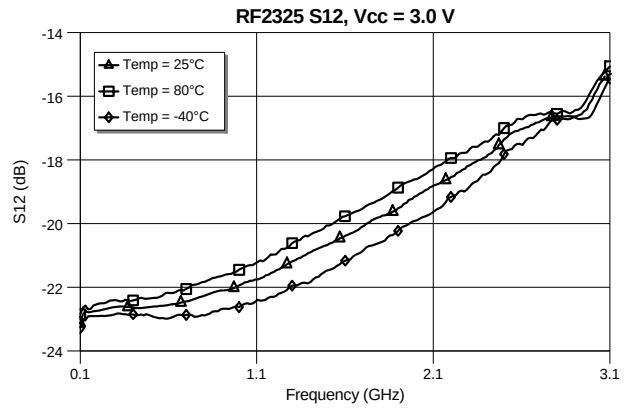
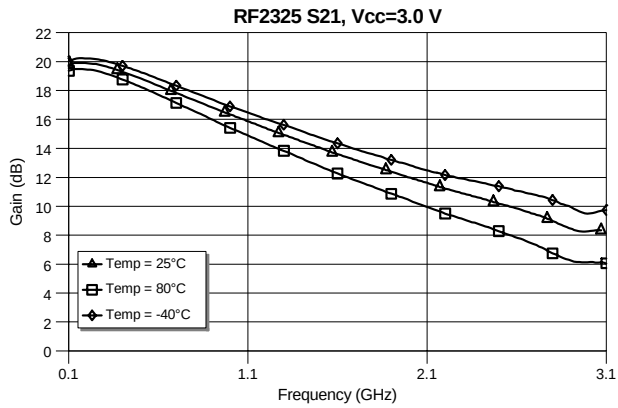


RF2325 S11, Vcc = 2.7 V, Temp = 25°C

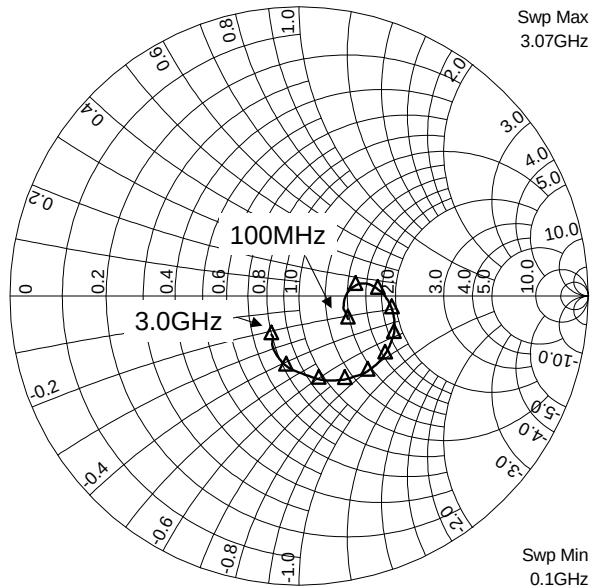


RF2325 S22, Vcc = 2.7 V, Temp= 25°C

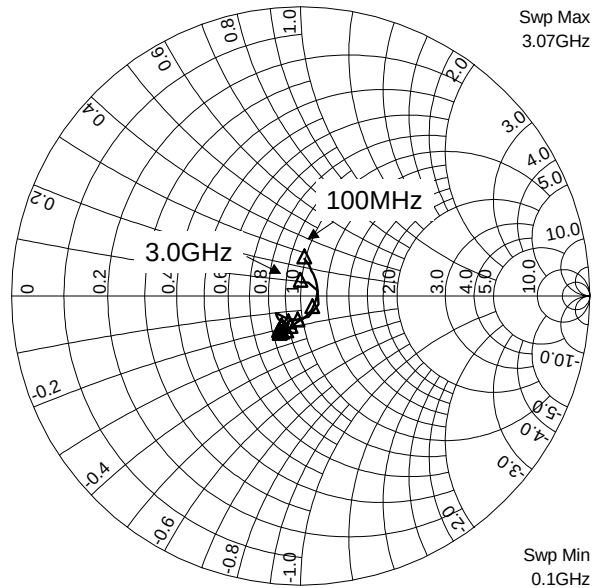


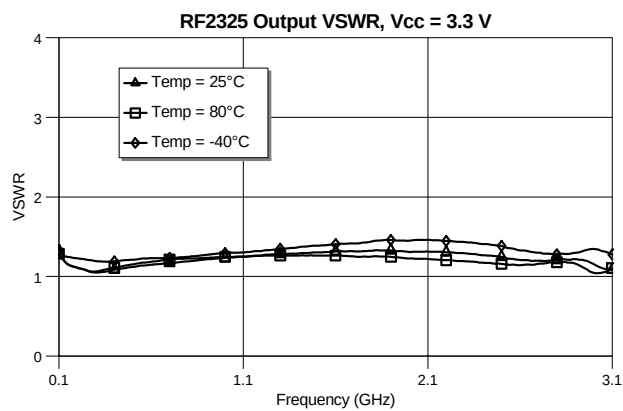
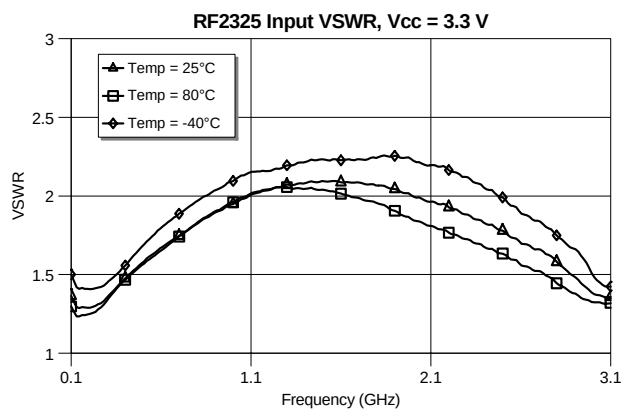
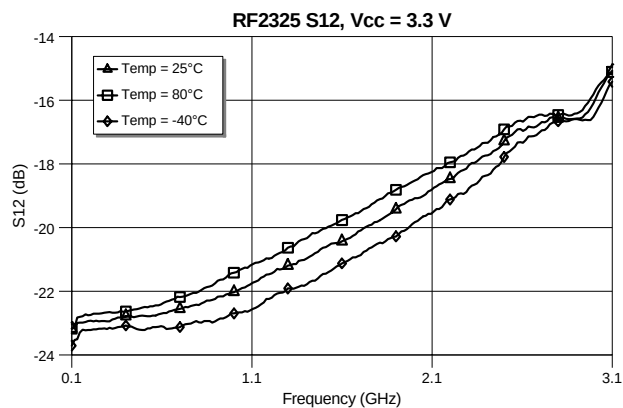
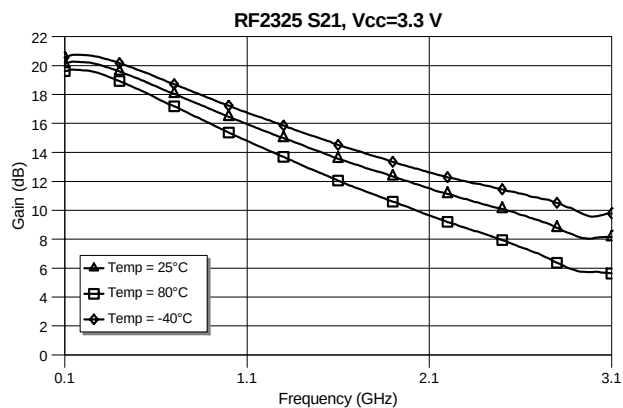


RF2325 S11, Vcc = 3.0 V, Temp = 25°C

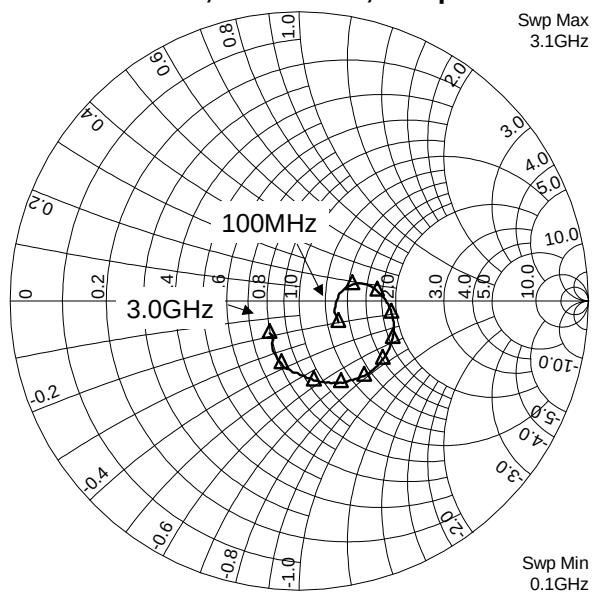


RF2325 S22, Vcc = 3.0 V, Temp= 25°C





RF2325 S11, Vcc = 3.3 V, Temp = 25°C



RF2325 S22, Vcc = 3.3 V, Temp= 25°C

