MRF161

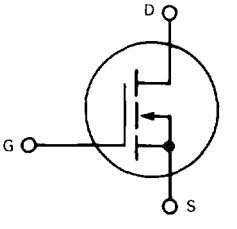
The RF MOSFET Line

2

N-CHANNEL ENHANCEMENT-MODE
RF POWER FIELD-EFFECT TRANSISTOR

. . . designed for wideband large-signal amplifier and oscillator applications in the 2.0 to 400 MHz range.

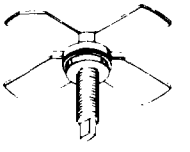
- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 5.0 Watts
  Minimum Gain = 11 dB
  Efficiency = 50% (Typical)
- Small-Signal and Large-Signal Characterization
- 100% Tested for Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 3.0 dB (Typ) at 100 mA, 400 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques

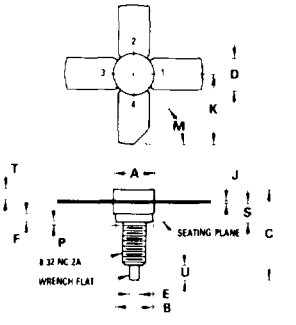


5.0 W 2.0–400 MHz

N-CHANNEL MOS
BROADBAND RF POWER

FET





STYLE 3
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	—	0.060	—
J	0.08	0.17	0.003	0.007
K	11.05	—	0.435	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.77	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	0.9	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	17.5 0.10	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

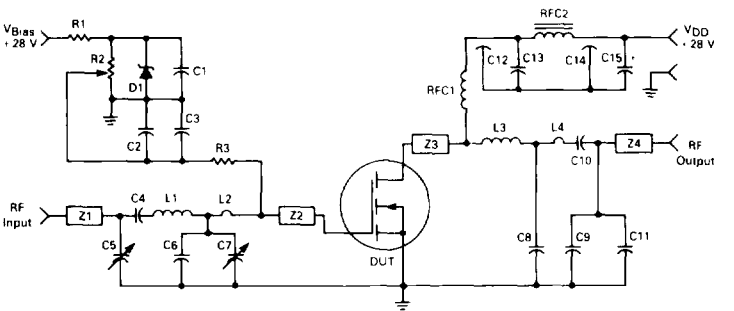
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 100 mA)	g_{fs}	80	110	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	7.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	9.7	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.3	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DS} = 28 Vdc, I_D = 100 mA, f = 400 MHz, Z_S = 67.6 + j14.1, Z_L = 14.5 + j25.7)	NF	—	3.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 400 MHz, I_{DQ} = 50 mA)	G_{ps}	11	13.5	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 400 MHz, I_{DQ} = 50 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 400 MHz, I_{DQ} = 50 mA, VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 400 MHz TEST CIRCUIT



C1, C2, C13 — 0.1 μF, 50 V Disc Ceramic
C3 — 0.01 μF, 100 V Disc Ceramic
C4, C10 — 220 pF, 100 Mil Chip Cap
C5 — 1–10 pF Johanson or Equivalent
C6 — 5.0 pF Mini-Unieco or Equivalent
C7 — 1–20 pF Johanson or Equivalent
C8 — 15 pF, 100 Mil ATC Chip Cap or Equivalent
C9, C11 — 2.2, 100 Mil ATC Chip Cap or Equivalent
C12, C14 — 680 pF Feedthru
C15 — 50 μF, 35 V
R1 — 1.6 kΩ, 1/4 W
R2 — 10 Turns 10 kΩ
R3 — 10 k, 1/2 W
D1 — 1N5347B Motorola Zener or Equivalent

L1 — 1-3/4 Turns, 0.185" ID 0.08" Long #20 AWG Enamel — (25 nH)
L2 — #20 AWG Enamel, Hairpin 0.353" — (10.5 nH) 0.185"
L3 — 1-3/4 Turns, 0.128" ID 0.11" Long #18 AWG Enamel — (15 nH)
L4 — #18 AWG Enamel, Hairpin 0.410" — (12.5 nH) 0.185"
RFC1 — 10 Turns, 0.300" ID #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK-200
Z1 — 0.82" x 0.164" Microstrip — (Z_O 50 Ω)
Z2, Z3 — 0.60" x 0.25" Microstrip
Z4 — 0.76" x 0.164" Microstrip — (Z_O 50 Ω)
Board-Glass Teflon, 62 Mils, ϵ_r 2.56

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FIGURE 2 — OUTPUT POWER versus INPUT POWER

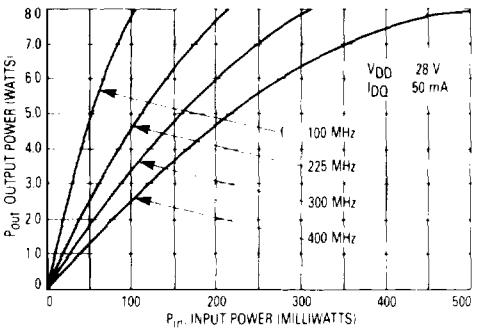


FIGURE 3 — OUTPUT POWER versus INPUT POWER

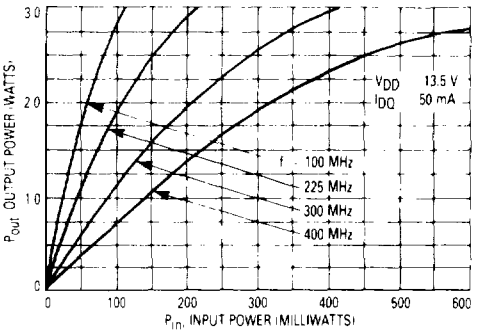


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

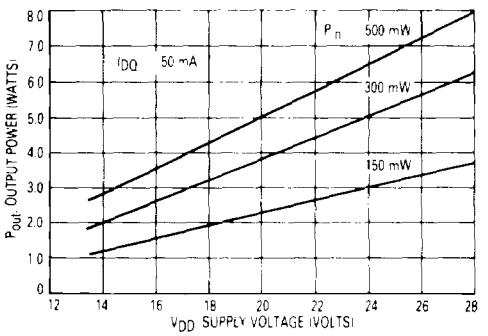


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 300 MHz

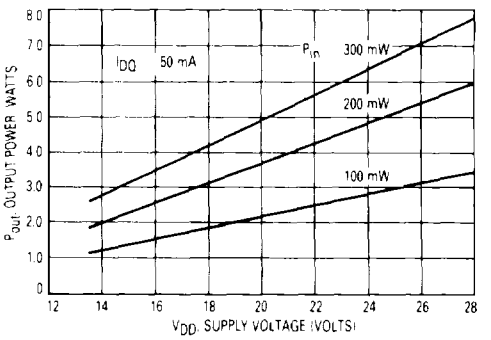


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 225 MHz

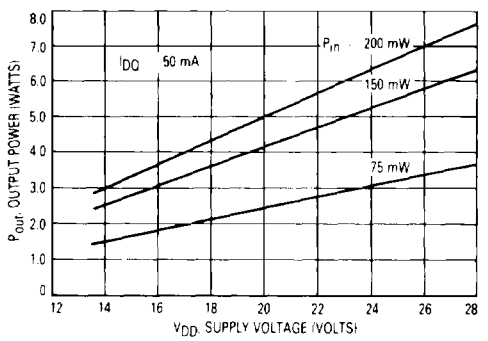


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

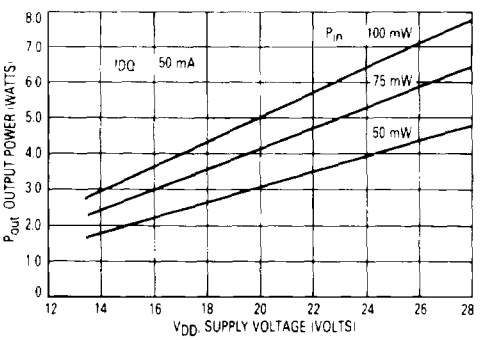


FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

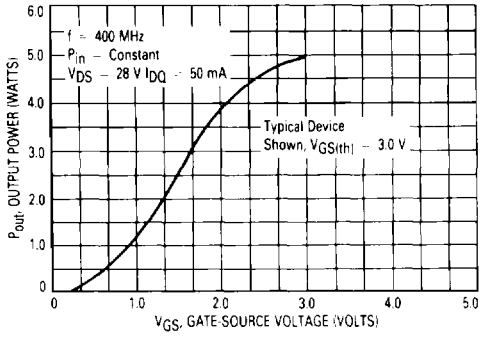


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

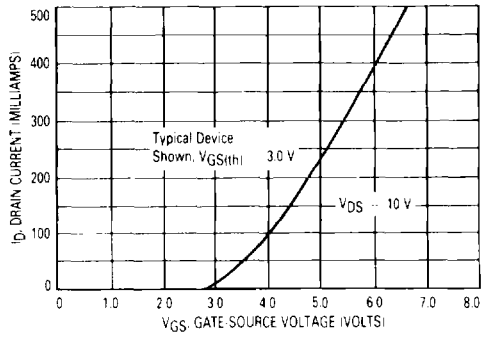


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

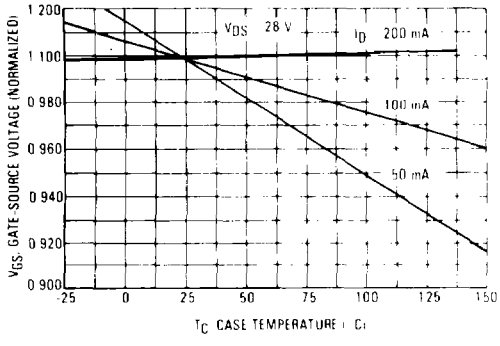


FIGURE 11 — CAPACITANCE versus VOLTAGE

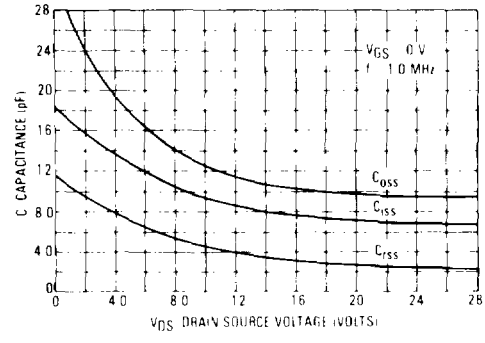


FIGURE 12 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

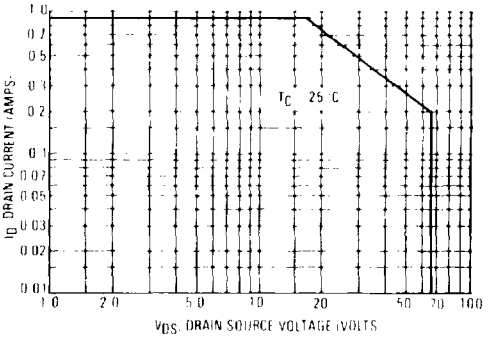
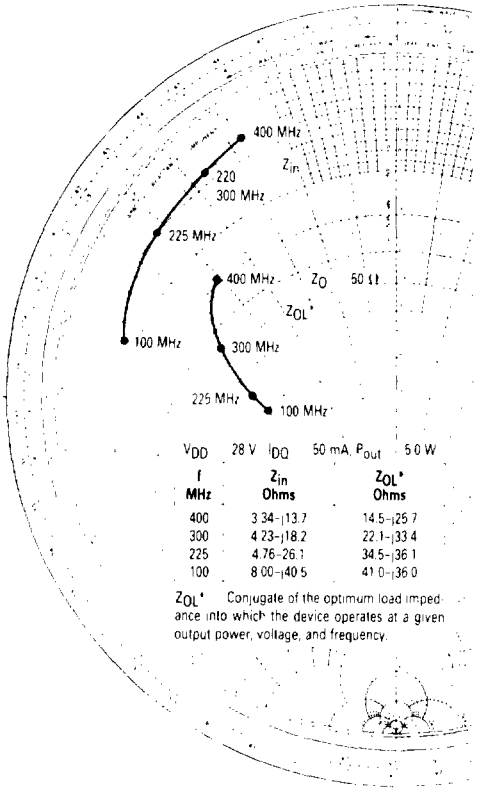


FIGURE 13 — LARGE-SIGNAL SERIES EQUIVALENT INPUT AND OUTPUT IMPEDANCE, Z_{in}, Z_{OL}*



V_{DD} 28 V, I_{DQ} 50 mA, P_{out} 5.0 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
400	3.34–j13.7	14.5–j25.7
300	4.23–j18.2	22.1–j33.4
225	4.76–26.1	34.5–j36.1
100	8.00–j40.5	41.0–j36.0

Z_{OL}* Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 14 — COMMON SOURCE SCATTERING PARAMETERS
50 OHM SYSTEM
V_{DS} = 28 V, I_D = 250 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	1.000	-1.69	13.64	178	0.002	62	0.947	-1.84
5.0	1.000	-4.63	13.60	176	0.005	69	0.945	-4.00
10	0.997	-8.95	13.70	173	0.010	80	0.941	-7.92
20	0.989	-17.49	13.36	167	0.022	73	0.929	-15.8
30	0.977	-26	13.07	162	0.032	71	0.915	-23
40	0.968	-34	12.76	156	0.042	67	0.902	-30
50	0.949	-42	12.31	151	0.050	61	0.885	-37
60	0.930	-49	11.88	146	0.058	57	0.866	-43
70	0.913	-56	11.45	141	0.066	53	0.846	-49
80	0.897	-62	10.96	137	0.072	50	0.831	-55
90	0.885	-68	10.50	133	0.078	46	0.817	-60
100	0.867	-74	10.00	129	0.081	43	0.800	-65
110	0.853	-78	9.54	125	0.085	40	0.787	-69
120	0.838	-84	8.92	122	0.090	37	0.775	-74
130	0.819	-88	8.75	119	0.093	35	0.762	-78
140	0.812	-92	8.30	116	0.096	31	0.755	-81
150	0.800	-96	7.95	113	0.098	28	0.742	-86
160	0.785	-99	7.54	111	0.100	26	0.735	-89
170	0.775	-103	7.25	109	0.102	24	0.728	-93
180	0.765	-105	6.85	106	0.103	23	0.725	-96
190	0.755	-108	6.60	104	0.104	21	0.720	-98
200	0.740	-111	6.20	100	0.106	18	0.719	-99
225	0.735	-116	5.71	96	0.110	16	0.715	-103
250	0.723	-121	5.17	92	0.112	12	0.708	-107
275	0.720	-124	4.80	89	0.113	10	0.706	-110
300	0.716	-128	4.43	85	0.112	7.0	0.706	-113
325	0.715	-130	4.17	83	0.111	4.0	0.717	-115
350	0.715	-133	3.87	79	0.111	3.0	0.720	-117
375	0.715	-135	3.67	76	0.111	1.0	0.728	-118
400	0.711	-137	3.43	74	0.109	0	0.729	-119
425	0.714	-139	3.25	71	0.104	0	0.738	-120
450	0.717	-140	3.11	69	0.104	-2.0	0.743	-121
475	0.719	-141	2.95	67	0.103	-3.0	0.757	-122
500	0.722	-142	2.81	65	0.102	-4.0	0.770	-122
525	0.723	-144	2.69	62	0.099	6.0	0.777	-123
550	0.727	-144	2.55	61	0.097	-6.0	0.787	-123
575	0.729	-145	2.46	59	0.097	-7.0	0.802	-124
600	0.733	-146	2.37	57	0.094	-7.0	0.814	-124
625	0.734	-147	2.29	55	0.090	-8.0	0.824	-126
650	0.740	-148	2.19	54	0.087	-8.0	0.830	-127
675	0.749	-149	2.12	53	0.085	-6.0	0.849	-127
700	0.758	-149	2.07	51	0.084	-6.0	0.879	-127
725	0.761	-150	1.99	49	0.082	-5.0	0.886	-127
750	0.763	-151	1.93	48	0.081	-4.0	0.905	-127
775	0.765	-151	1.90	48	0.079	-3.0	0.919	-128
800	0.770	-152	1.83	46	0.076	-1.0	0.921	-128

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FIGURE 15 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 250 mA

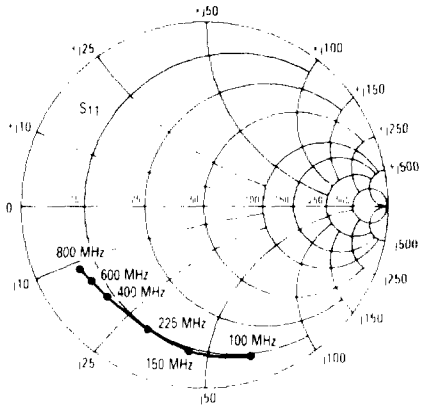


FIGURE 16 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 250 mA

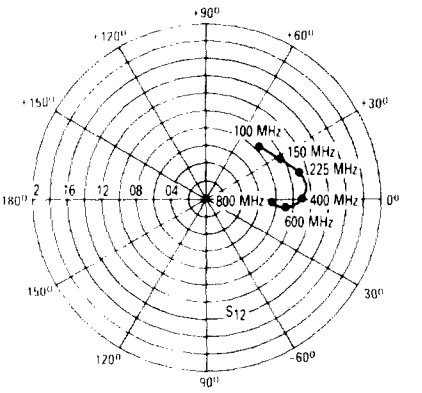


FIGURE 17 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 250 mA

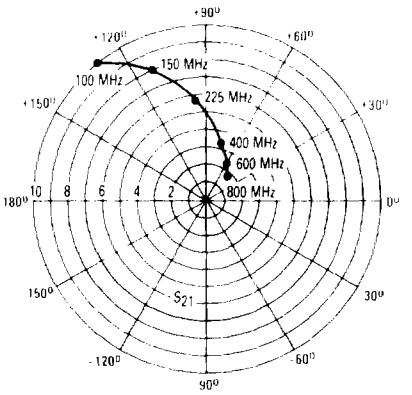
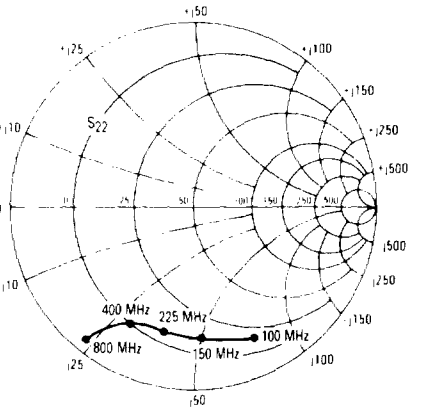


FIGURE 18 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{OS} = 28 V, I_D = 250 mA



DESIGN CONSIDERATIONS

The MRF161 is a RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for UHF power amplifier and oscillator applications. Motorola RF MOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF161 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF161 was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF161 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar UHF transistors are suitable for the MRF161. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF161, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF161 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A for a discussion of two port network theory and stability.

FIGURE 19 — 400 MHz TEST CIRCUIT