

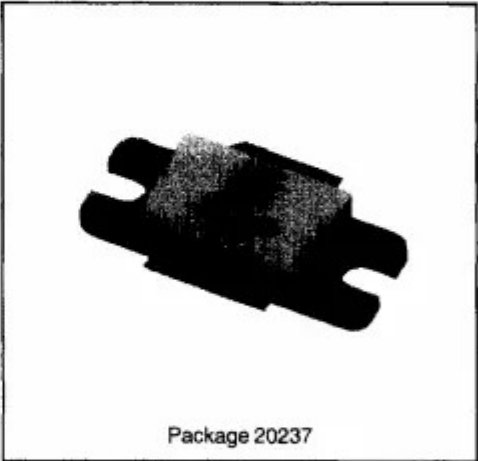
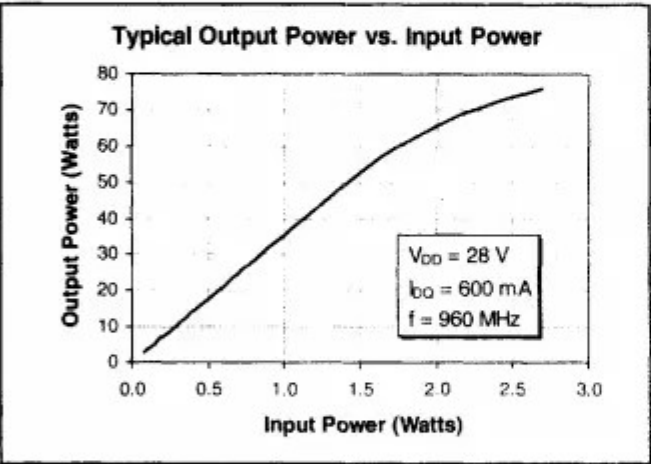
PTE 10019*
70 Watts, 860–960 MHz
LDMOS Field Effect Transistor

Description

The 10019 is an internally matched common source n-channel enhancement-mode lateral MOSFET intended for cellular, GSM, and DAMP applications in the 860 to 960 MHz range. It is rated at 70 watts minimum output power. Nitride surface passivation and gold metallization ensure excellent device lifetime and reliability. 100% lot traceability is standard.

- Input **INTERNALLY MATCHED** for ease of circuit design
- Performance at 960 MHz, 28 Volts
 - Output Power = 70 Watts
 - Power Gain = 14.5 dB Typ
 - Efficiency = 50% Typ
- Gold Metallization
- Silicon Nitride Passivated
- Excellent Thermal Stability

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Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation at $T_{flange} = 25^{\circ}C$ Above $25^{\circ}C$ derate by	P_D	215 1.25	Watts W/°C
Storage Temperature Range	T_{STG}	-40 to +150	°C
Thermal Resistance ($T_{flange} = 70^{\circ}C$)	$R_{\theta JC}$	0.8	°C/W

* A "PTE" number indicates that specification is preliminary and subject to change. Order this product or obtain additional information from your Ericsson Sales Representative.

PTE 10019



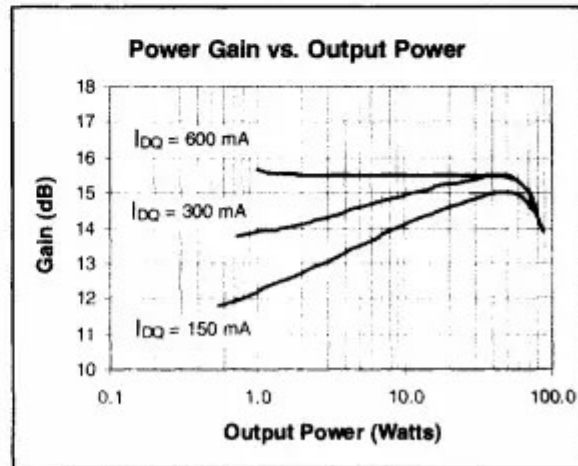
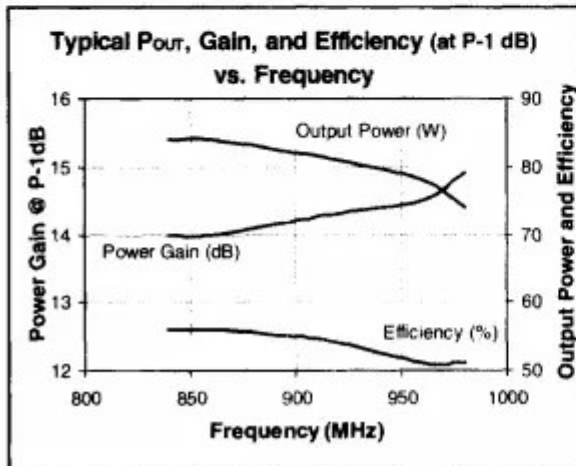
Electrical Characteristics (100% Tested)

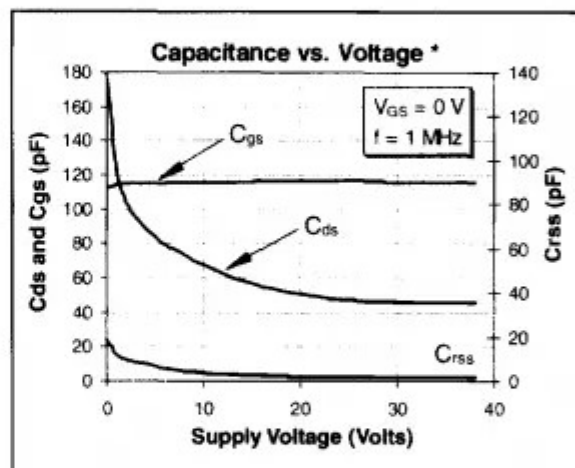
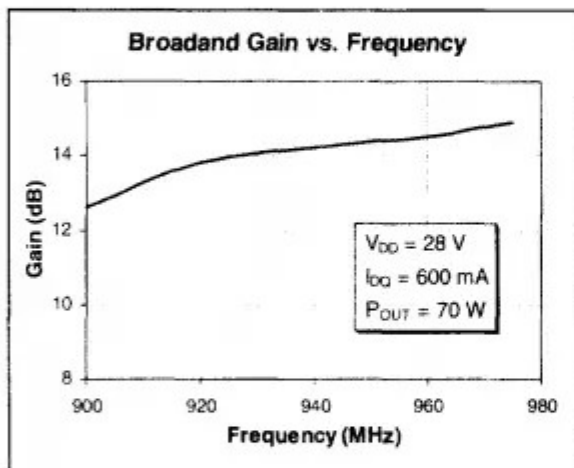
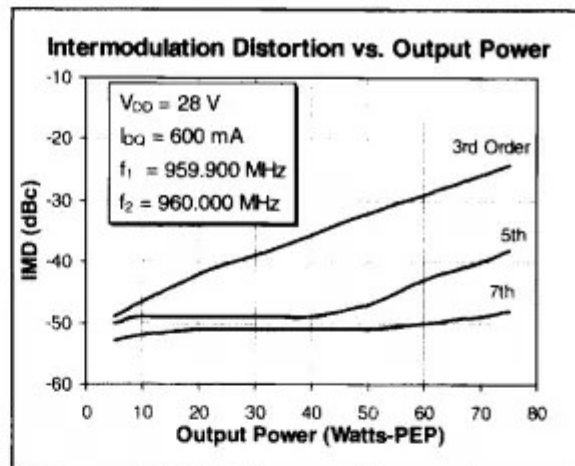
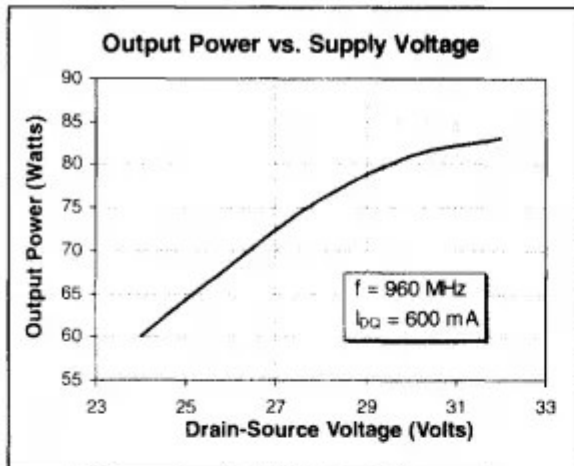
Characteristic	Conditions	Symbol	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 25\text{ mA}$	$V_{(BR)DSS}$	65	—	—	Volts
Drain-Source Leakage Current	$V_{DS} = 26\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	mA
Gate Threshold Voltage	$V_{DS} = 10\text{ V}$, $I_D = 75\text{ mA}$	$V_{GS(th)}$	—	2.0	—	Volts
Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 3\text{ A}$	g_{fs}	—	3.0	—	Siemens

RF Specifications (100% Tested)

Characteristic	Symbol	Min	Typ	Max	Units
Gain ($V_{DD} = 28\text{ V}$, $P_{out} = 70\text{ W}$, $I_{DQ} = 600\text{ mA}$, $f = 960\text{ MHz}$)	G_{pe}	13.0	14.5	—	dB
Drain Efficiency ($V_{DD} = 28\text{ V}$, $P_{out} = 70\text{ W}$, $I_{DQ} = 600\text{ mA}$, $f = 960\text{ MHz}$)	η	45	50	—	%
Load Mismatch Tolerance ($V_{DD} = 28\text{ V}$, $P_{out} = 70\text{ W}$, $I_{DQ} = 600\text{ mA}$, $f = 960\text{ MHz}$ —all phase angles at frequency of test)	ψ	—	—	10:1	—

Typical Performance

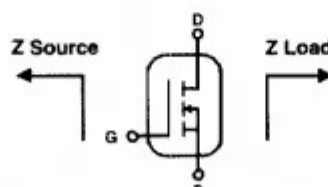




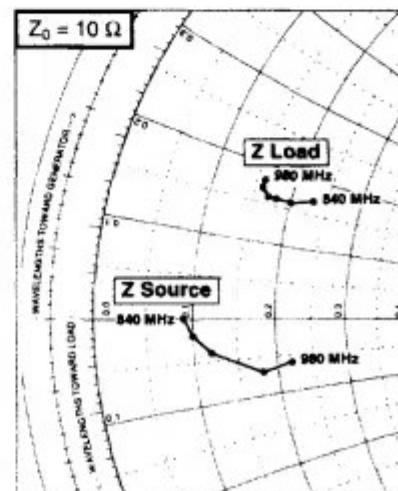
* This part is internally matched. Measurements of the finished product will not yield these figures.

Impedance Data

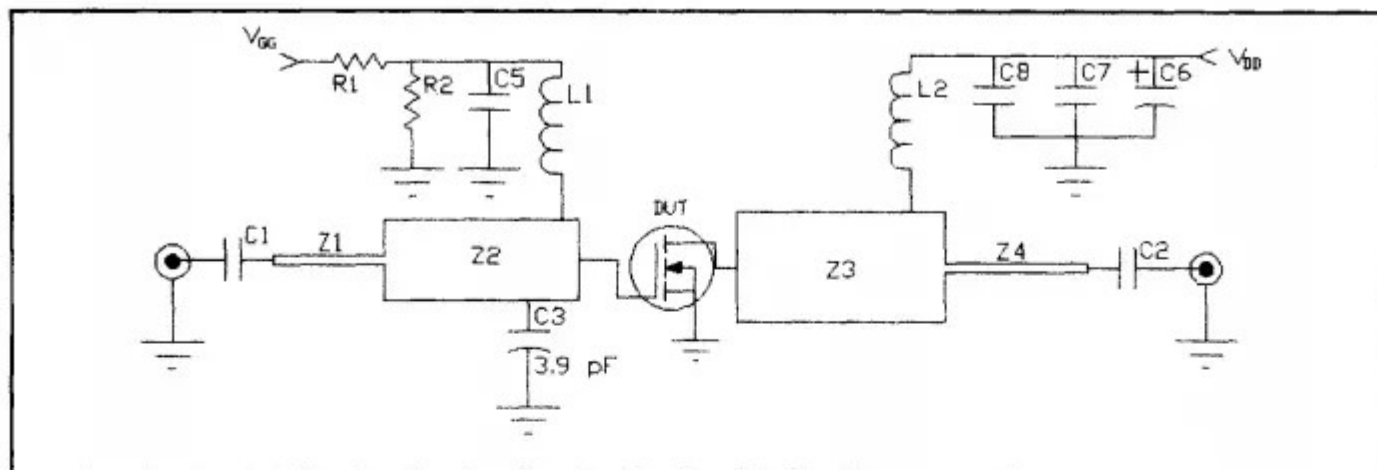
$V_{DD} = 28 \text{ V}$, $P_{out} = 70 \text{ W}$, $I_{DQ} = 600 \text{ mA}$



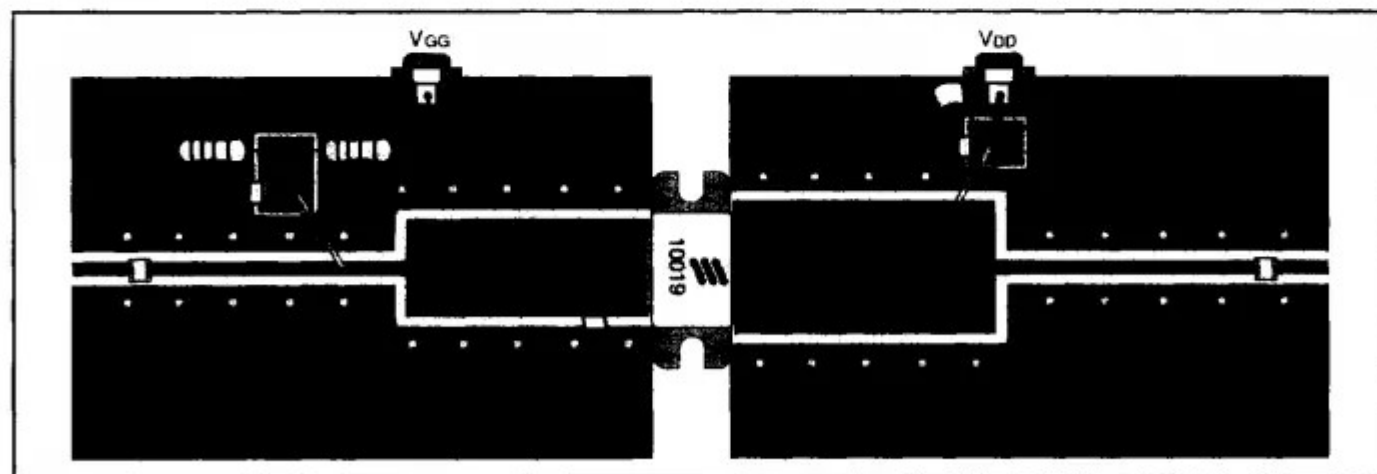
Frequency MHz	Z Source		Z Load	
	R	jX	R	jX
840	0.9	0	2.3	1.7
860	1.0	-0.2	2.0	1.6
900	1.2	-0.4	1.8	1.6
920	1.2	-0.4	1.7	1.6
960	1.8	-0.7	1.6	1.7
980	2.2	-0.6	1.6	1.8



Test Circuit

Test Circuit Schematic for $f = 960$ MHz

DUT	10019	LDMOS Field Effect Transistor	L1, L2	4 Turn, #20 AWG, .120" I.D.
Z1, Z4		Microstrip 50 Ω	R1, R2	2.2 K, 1/4 W Resistor
Z2	0.19 λ 960 GHz	Microstrip 10.2 Ω	Circuit Board	0.031" thick, $\epsilon_r = 4.0$, AlliedSignal, G200
Z3	0.21 λ 960 GHz	Microstrip 7.5 Ω		
C1	33 pF	Chip Cap ATC 100 B		
C2	43 pF	Chip Cap ATC 100 B		
C3	3.9 pF	Chip Cap ATC 100 B		
C5	43 pF	Chip Cap ATC 100 B		
C6	50 μ F, 35 V	Electrolytic Capacitor, Digi-Key P5276		
C7	0.1 μ F	Capacitor Digi-Key P4917-ND		
C8	43 pF	Chip Cap ATC 100 B		



Components Layout (not to scale)