300W, HF-0.5GHz 50V High Power RF LDMOS

Description

The SD2933LD is a 300W single ended 50V LDMOS, unmatched for any applications within HF-0.5GHz

It supports CW, and pulsed and any modulated signal at either saturated or linear application.

It can be the drop-in replacement of its equivalent 300W single ended VDMOS like SD2933/VRF2933 with improved RF performance like higher efficiency

Typical performance(on test board with device soldered)
Signal: CW , Vgs=3.35v,Vds=50v,Idq=200mA

| Freq(MHz) | Pin(dBm) | Pout(dBm) | Pout(W) | lds(A) | Gain(dB) | Eff(%) | 2 nd | 3 rd |
|-------------|-------------|-------------|----------|--------|-----------|--------|-----------------|-----------------|
| Freq(IVIH2) | Pili(ubili) | Pout(dBill) | Poul(vv) | ius(A) | Gairi(ub) | | Harmonic(dB) | Harmonic(dB) |
| 30 | 33.2 | 55.6 | 350 | 9.5 | 24 | 74 | -27 | -39 |

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- · Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

| Rating | Symbol | Value | Unit |
|--------------------------------|------------------------------|-------------|------|
| DrainSource Voltage | $V_{\scriptscriptstyle DSS}$ | +135 | Vdc |
| GateSource Voltage | V_{GS} | -10 to +10 | Vdc |
| Operating Voltage | V_{DD} | +55 | Vdc |
| Storage Temperature Range | Tstg | -65 to +150 | °C |
| Case Operating Temperature | Tc | +150 | °C |
| Operating Junction Temperature | TJ | +225 | °C |

Table 2. Thermal Characteristics

| Characteristic | Symbol | Value | Unit | |
|---|--------|-------|------|--|
| Thermal Resistance, Junction to Case | Dolo | 0.5 | 0000 | |
| T _C = 85°C, T _J =200°C, DC test | RөJC | 0.5 | °C/W | |

Table 3. ESD Protection Characteristics

| Test Methodology | Class |
|-----------------------------------|---------|
| Human Body Model (per JESD22A114) | Class 2 |

Table 4. Electrical Characteristics (T_A = 25 °C unless otherwise noted)

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| Characteristic | Symbol | Min | Тур | Max | Unit |
|---|----------------------|---------------------|------|-----|------|
| DC Characteristics | | | | | |
| Drain-Source Voltage | V _{(BR)DSS} | | 135 | | V |
| V _{GS} =0, I _{DS} =1.0mA | V (BR)DSS | | 133 | | V |
| Zero Gate Voltage Drain Leakage Current | | l _{DSS} —— | | 1 | |
| $(V_{DS} = 75V, V_{GS} = 0 V)$ | IDSS | | | | μА |
| Zero Gate Voltage Drain Leakage Current | | | | 1 | ^ |
| $(V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V})$ | I _{DSS} | | | | μА |
| GateSource Leakage Current | | | | 4 | |
| $(V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V})$ | I _{GSS} | | | 1 | μΑ |
| Gate Threshold Voltage | V (II) | | 2.65 | | V |
| $(V_{DS} = 50V, I_D = 600 \mu A)$ | V _{GS} (th) | | | | |
| Gate Quiescent Voltage | V | | 3.4 | | V |
| (V_{DD} = 50 V, I_{D} = 200 mA, Measured in Functional Test) | $V_{GS(Q)}$ | | | | V |
| Drain source on state resistance | Rds(on) | | 180 | | mΩ |
| (Vds=0.1V, Vgs=10V) | Rus(on) | | 100 | | |
| Common Source Input Capacitance | C _{ISS} | | 220 | | pF |
| $(V_{GS} = 0V, V_{DS} = 50 V, f = 1 MHz)$ | Ciss | | 220 | | pΓ |
| Common Source Output Capacitance | C _{oss} | | 65 | | pF |
| $(V_{GS} = 0V, V_{DS} = 50 V, f = 1 MHz)$ | Coss | | 00 | | þΓ |
| Common Source Feedback Capacitance | 6 | | 1.5 | | n.E |
| $(V_{GS} = 0V, V_{DS} = 50 V, f = 1 MHz)$ | C _{RSS} | | 1.5 | | pF |

Load Mismatch (Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 200 mA, f = 108MHz, pulse width:100us, duty cycle:10%

| Load 20:1 All phase angles, at 350W Pulsed CW Output Power | No Device Degradation |
|--|-----------------------|
|--|-----------------------|

TYPICAL CHARACTERISTICS

Figure 1: CW Gain and Power Efficiency as a Function of Pout at 30MHz

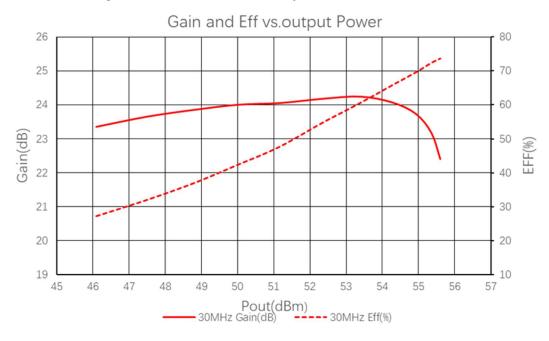


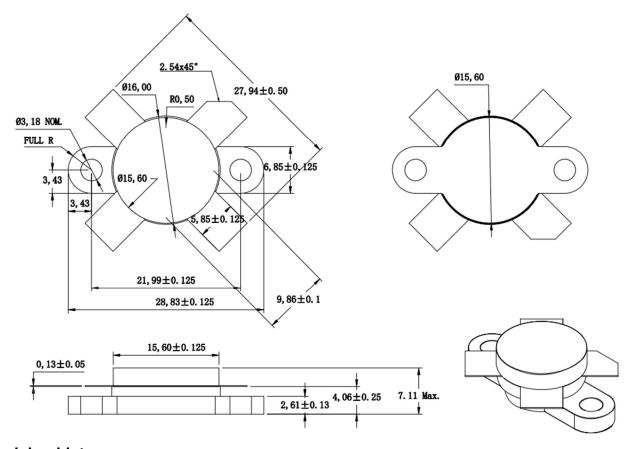
Figure 2: Class C, Low Bias, Low Power Input (0 dBm) S11 / S21



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Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads (1—Gate, 2—Drain, 3—Source)



Revision history

Table 5. Document revision history

| | <u> </u> | |
|------------|----------|---|
| Date | Revision | Datasheet Status |
| 2021/6/22 | Rev 1.0 | Preliminary datasheet |
| 2022/5/24 | Rev 1.1 | Modification of V4E package picture and drawing |
| 2023/11/21 | Rev 2.0 | Modify drawing of extended leads length |
| 2023/12/4 | Rev 3.0 | Finalized by changing to V4E1 package |

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