SD2933LD LDMOS RF TRANSISTOR

Part Number: SD2933LD
Datasheet V3.0

300W, HF-0.5GHz 50V High Power RF LDMOS

SD2933LD

Description

The SD2933LD is a 300W single ended 50V LDMOS, unmatched for any applications within HF-0.5GHz

It supports CW, and pulsed and any modulated signal at either saturated or linear application.

It can be the drop-in replacement of its equivalent 300W single ended VDMOS like SD2933/VRF2933 with improved RF performance like higher efficiency

- Typical performance(on test board with device soldered)

  Signal: CW , Vgs=3.35v,Vds=50v,Idq=200mA

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	Ids(A)	Gain(dB)	Eff(%)	2nd Harmonic(dB)	3rd Harmonic(dB)
30	33.2	55.6	350	9.5	24	74	-27	-39

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+135	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	0.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS}(th)$	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.4	——	V
Drain source on state resistance (Vds=0.1V, Vgs=10V)	Rds(on)		180		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}		220		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}		65		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}		1.5		pF

Load Mismatch (Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 200 mA, f =108MHz, pulse width:100us, duty cycle:10%

Load 20:1 All phase angles, at 350W Pulsed CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1: CW Gain and Power Efficiency as a Function of Pout at 30MHz

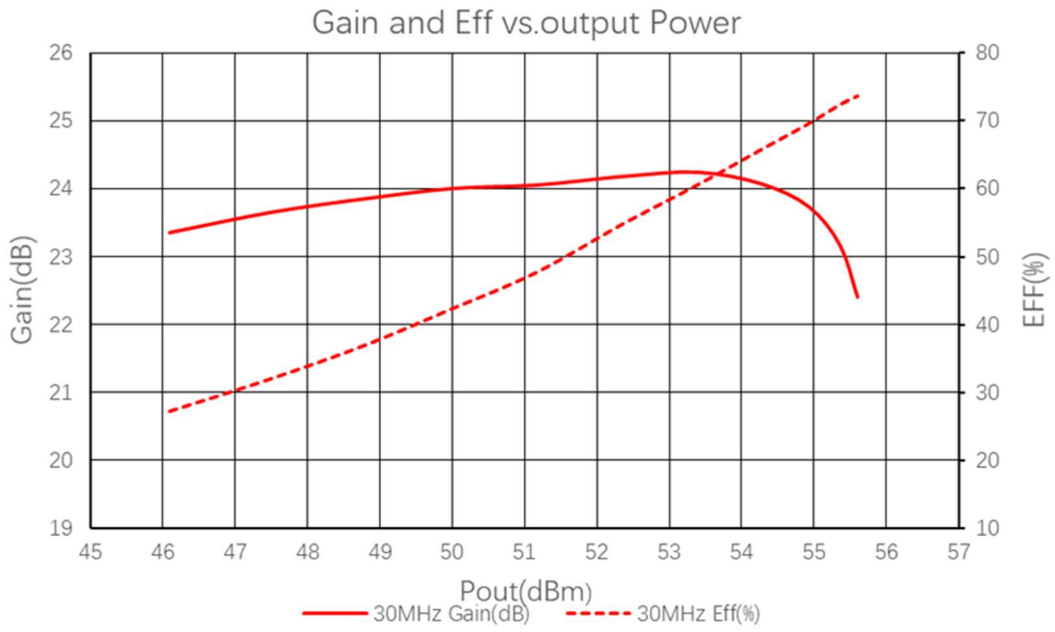
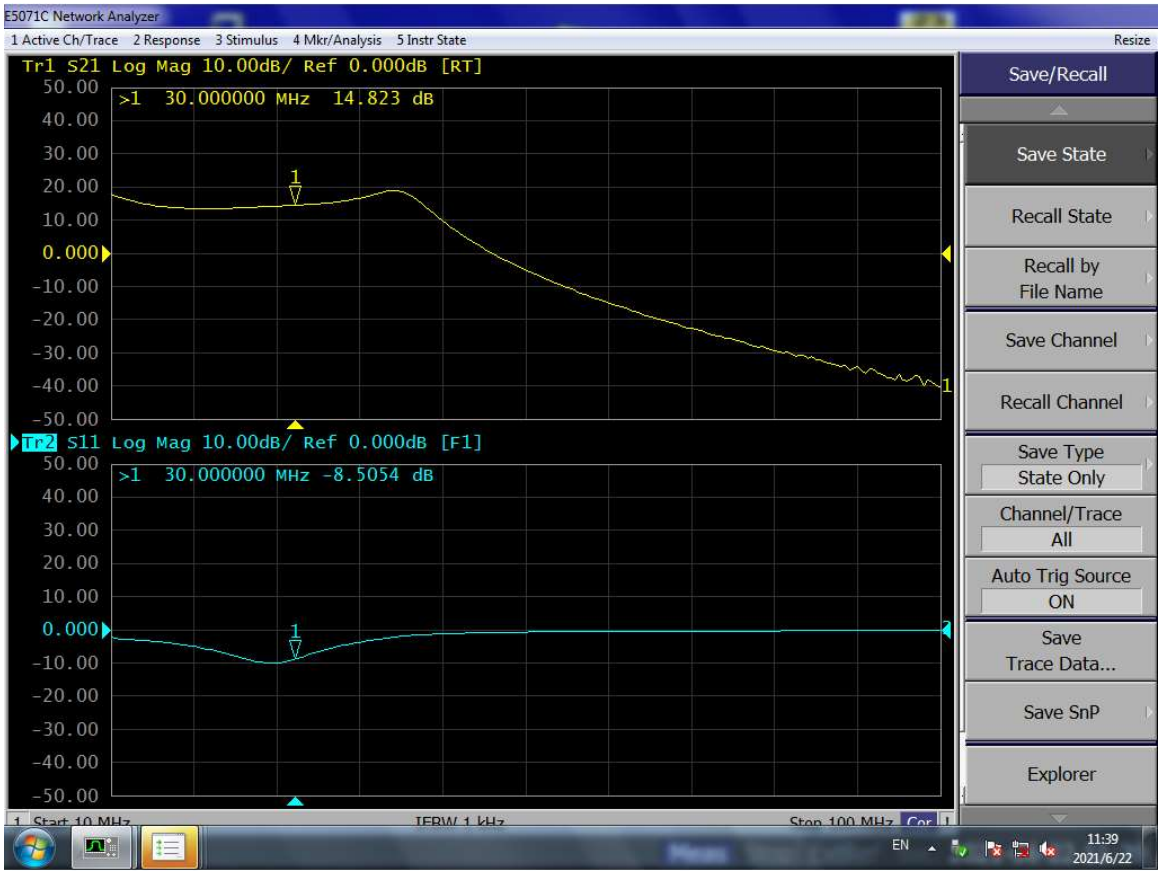
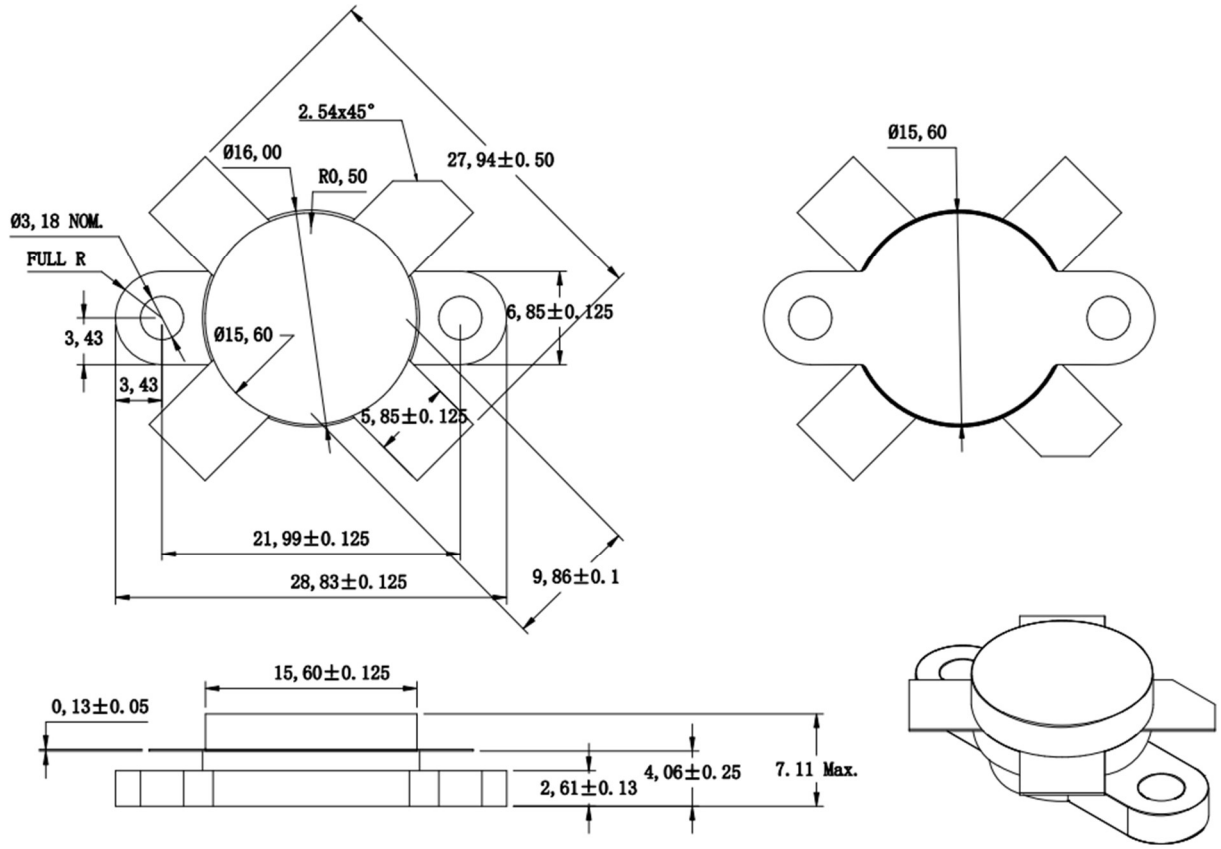


Figure 2: Class C, Low Bias, Low Power Input (0 dBm) S11 / S21



Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads（1—Gate、2—Drain、3—Source）



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/6/22	Rev 1.0	Preliminary datasheet
2022/5/24	Rev 1.1	Modification of V4E package picture and drawing
2023/11/21	Rev 2.0	Modify drawing of extended leads length
2023/12/4	Rev 3.0	Finalized by changing to V4E1 package

Disclaimers